Interlock Builder User Guide

August 2023

Digital Dynamics, Inc | 5 Victor Square, Scotts Valley, CA 95066
Tel: 831-438-4444 | https://www.digitaldynamics.com

Contents

1 OVERVIEW

1.1 INTERLOCK BUILDER

The Interlock Builder™ application allows automation and machine system designers to implement software based, TÜV-certified safety interlocks for Fusion.IO systems. User defined interlocks control digital output states based on logic conditions which are applied to the state(s) of one or more digital inputs. Once designed, interlocks are programmed into a Fusion.IO system and their status can be monitored within Interlock Builder during testing.

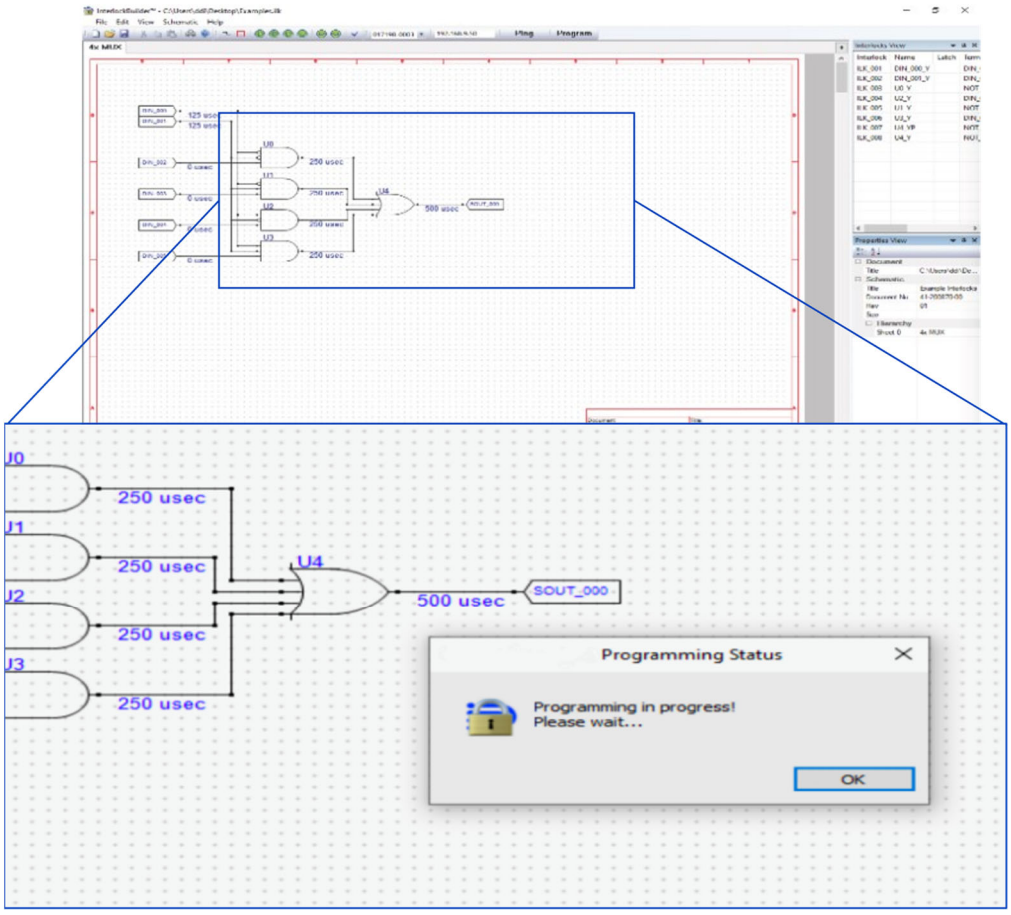


Figure 1-- Interlock Builder

Digital I/Os and logical conditions are available as blocks in Interlock Builder's schematic design environment which can be dropped into a schematic and wired together to create interlocks. Logical conditions which are available include:

- AND, OR, XOR gates
- Buffers
- Latches

Interlock Builder also provides protections to secure programmed interlocks and user data such as:

- AES 256-bit encryption and RSA 4096-bit authentication of schematic project files and exported interlocks
- Robustness for handling communication and power interruption between the PC and Fusion device

- Tamper prevention of existing interlocks in a Fusion.IO system

1.2 FUSION.IO SYSTEM

A Fusion.IO system is an I/O control platform which is comprised of one Fusion device and one or more Remote Interface Module (RIM) devices. Each Fusion or RIM device is configured with a selection of user defined slot cards which provide a high density of digital and analog I/O channels as well as other channel types such as serial (RS232 and RS485), temperature measurement (thermocouple and resistance temperature detectors (RTD)), and relay output. The safety implementation of a Fusion.IO system allows I/O channels from one or more of its connected devices to be used when designing safety interlocks. For example, I/O channels from the main Fusion and one or more RIM devices can be combined into safety rated interlocks.

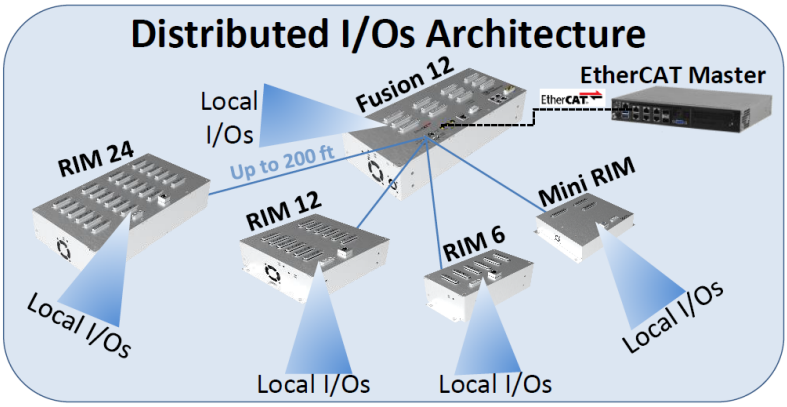


Figure 2-- Distributed Architecture

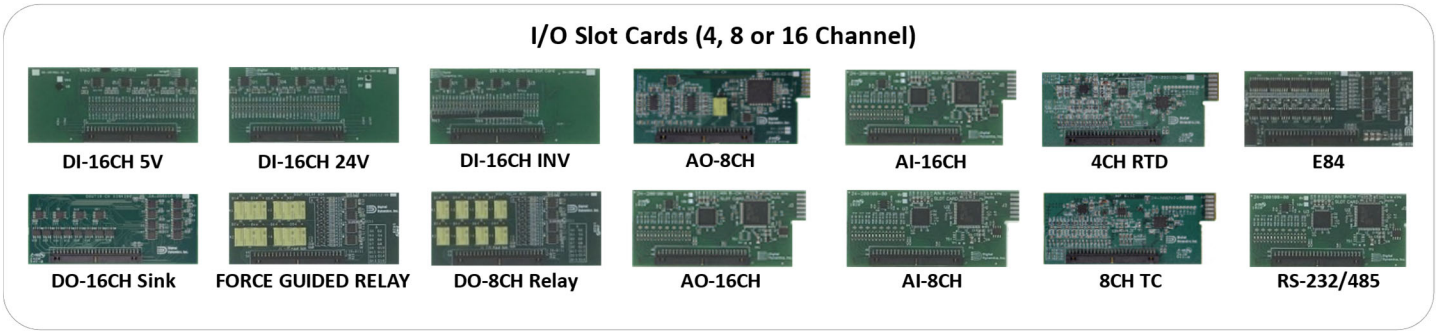


Figure 3 -- I/O Slot Cards

1.3 PROJECT ORGANIZATION

Interlock projects are saved as a single, encrypted file. Multiple schematic sheets can be created for projects, where each sheet is shown as a separate tab. Schematic sheets can be imported or exported. This helps you organize sections of interlocks by functional purpose, machine segments, etc. Project title, document number, revision, and names of individual schematic sheets can be assigned in the Properties View. Field Connects can be exported to unencrypted comma delimited (CSV) files. Schematics can be exported as schematic file or a bitmap.

1.4 FEATURES AND BENEFITS

EASE OF CONFIGURATION

Safety interlocks are quickly and easily designed and programmed using Interlock Builder's schematic design environment, eliminating lengthy hardware design cycles.

DISTRIBUTED SAFETY INTERLOCKS

I/Os used in interlocks can span across distributed Fusion and Remote Interface Module (RIM) systems while still allowing system designers to achieve Safety Integration Level SIL 3 safety functions.

INTRINSIC SECURITY

Encryption and tamper protection features are built into the core of Interlock Builder to secure both project files and interlock programming of Fusion systems.

ONLINE MONITORING

Status of all I/O channels are monitored while Interlock Builder is connected online with a Fusion system, allowing debugging of interlocks as well as testing and troubleshooting during system commissioning.

2 INSTALLATION

This chapter provides the system requirements and the installation instructions.

2.1 SYSTEM REQUIREMENTS

Your system needs to meet the following requirements to be able to install Interlock Builder.

2.1.1 Operating System Requirements

The following operating systems are supported:

- Windows 10 (32 or 64 bit)
- Windows 11 (64 bit)

2.1.2 Hardware Requirements

Interlock Builder requires the following:

- Interlock Builder requires 30MB of disk space
- Ethernet connection to the Fusion.IO system using a static IP address
- Static IP Address assign to PC network adapter which is compatible with the Fusion.IO system's IP address
    - A Fusion system's default IP is 192.168.9.50

2.2 DOWNLOADING THE SOFTWARE

Please contact Digital Dynamics for instructions to download the current version of Interlock Builder.

2.3 INSTALLING THE SOFTWARE

1. If an older version Interlock Builder is already installed, the existing version should first be uninstalled through the Windows Apps & Features settings:

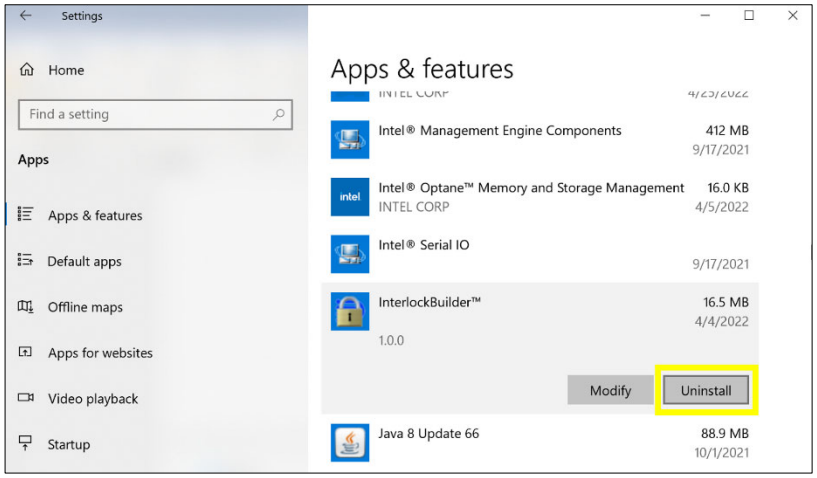


Figure 4 - Uninstall through Windows Apps & Features

2. Navigate to the folder where the Interlock Builder installation file is located.
3. Double-click the installation file “InterlockBuilder_vX.X.X.msi”.
4. After the Interlock Builder Setup window appears, click Next.

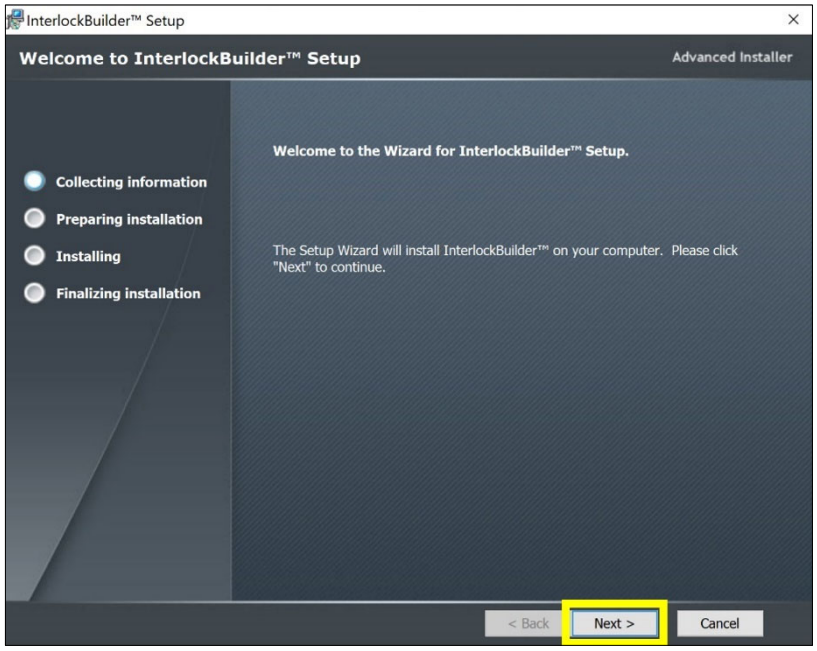


Figure 5 - Interlock Builder Setup

5. When the Installation Folder window appears, select the location where Interlock Builder should be installed, if you want to use a different location than the default. Click Next to continue.

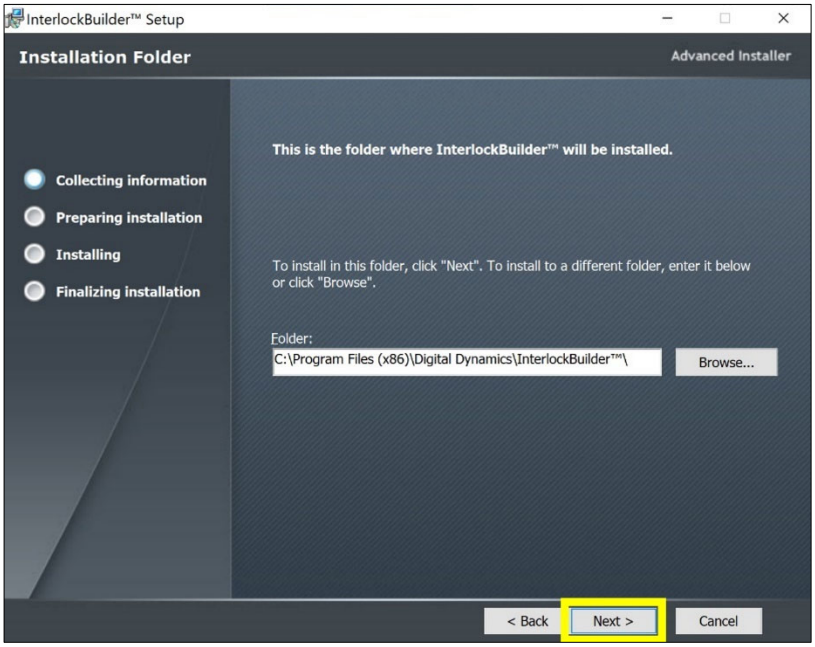


Figure 6 - Installation Location

6. After the Ready to Install window appears, click Install to start the installation.

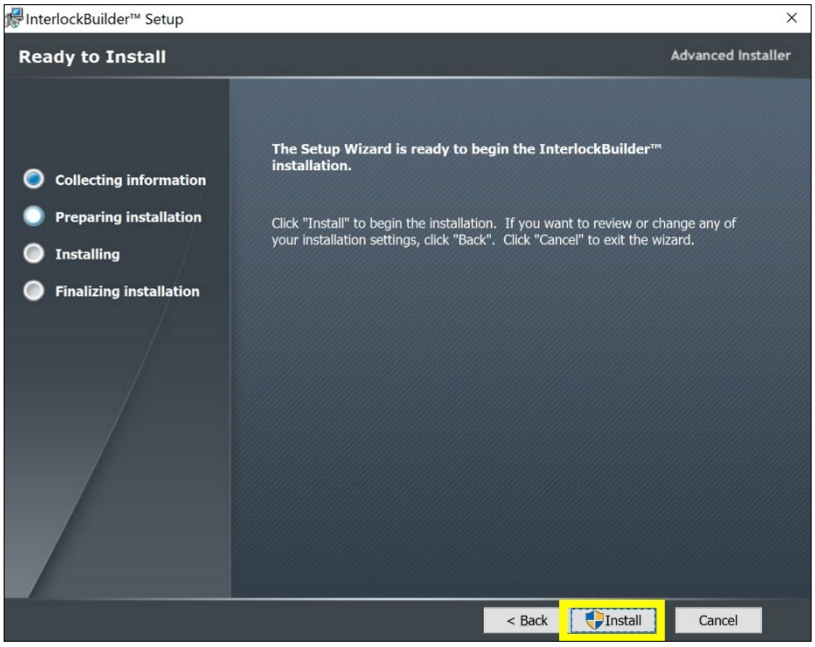


Figure 7 - Ready to Install

7. After the Interlock Builder Setup Complete window appears, click Finish to complete the installation process.

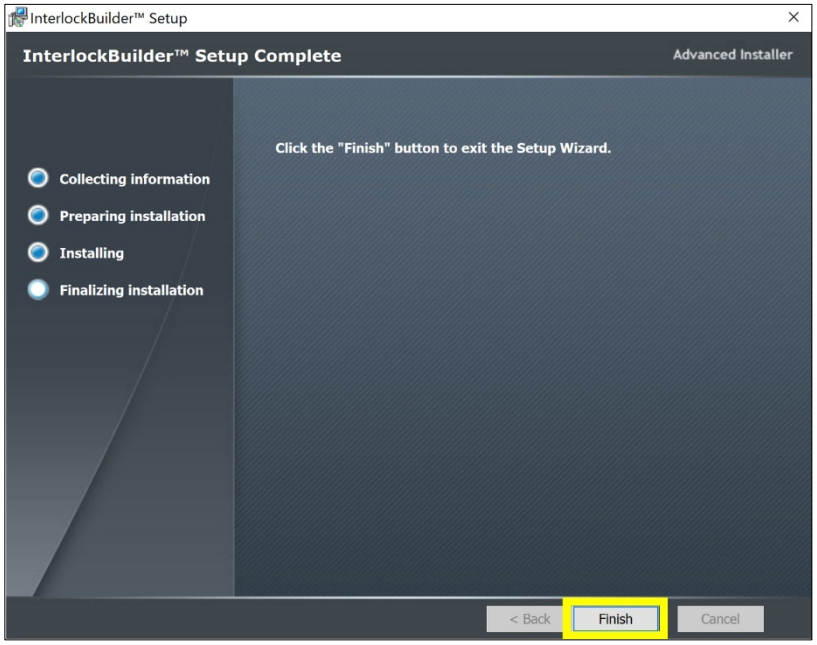


Figure 8 - Setup Complete

Interlock Builder is now available in from the Windows Start menu.

2.4 CONFIGURING THE STATIC IP ADDRESS

If your network environment uses dynamic IP addresses, you can set up a second static ethernet connection to the Fusion.IO system.

To set up a second ethernet adaptor in Windows 11

1. Add a USB to Ethernet connector to the computer used to control the Fusion.IO system. Use this connector to connect to the Fusion.IO system using the provided cable. Verify that the Ethernet jack status lights up.
2. Click the Windows button then navigate to Settings > Network & Internet > and click Advanced Network Settings.
3. Select the USB to ethernet adaptor. (It may say Ethernet Adapter #2.)
4. Scroll down and click View Additional Properties.
5. Click Edit next to IP Assignment and choose Manual.
6. Assign a static IP Address to USB to PC network adapter that is a value lower than the Fusion system's default IP address of 192.168.9.50. For example, you can set it to 192.168.9.40.

2.5 STARTING INTERLOCK BUILDER

To start using Interlock Builder, click the Interlock Builder Program in the Windows Start menu.

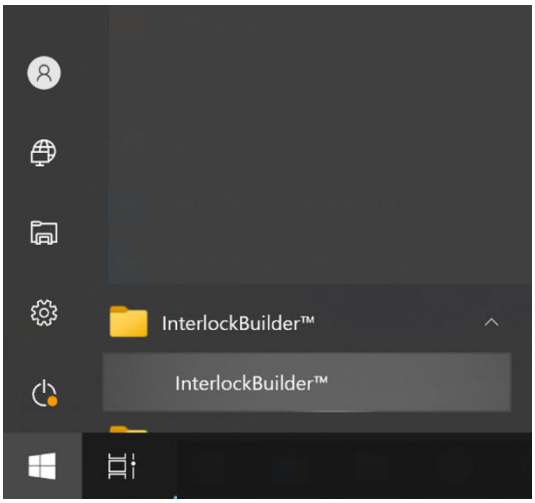


Figure 9 - Interlock Builder in Windows Start Menu

2.6 ADJUSTING THE DPI SETTINGS

If you are using high DPI displays, you may see issues with how the Interlock Builder user interface appears. For example, the size and clarity of UI elements such as text, toolbars, application icons, application windows, dialog boxes, etc., may need to be adjusted. If needed, you can change the Windows DPI settings for Interlock Builder.

To adjust the DPI settings:

1) Close Interlock Builder.
2) Right-click the application and select Properties.
3) Select the Compatibility tab and click the “Change high DPI settings” button (Figure 10 - Interlock Builder Application Properties).
4) Change the following High DPI scaling override settings (Figure 11 - High DPI Settings):
    a. Select “Override high DPI scaling behavior”.
    b. Set “Scaling Performed by” to “System”.
5) Run Interlock Builder and confirm that your display symptoms have been resolved.

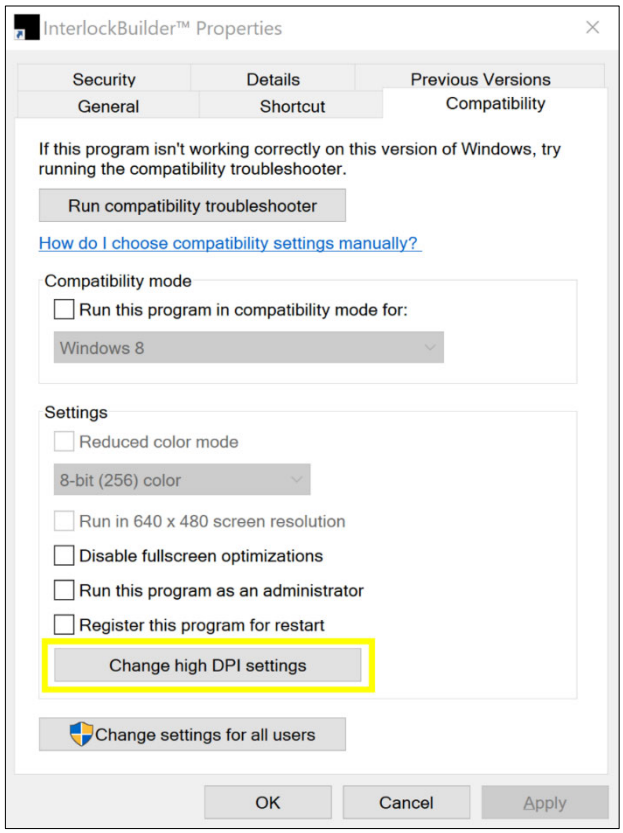


Figure 10 - Interlock Builder Application Properties

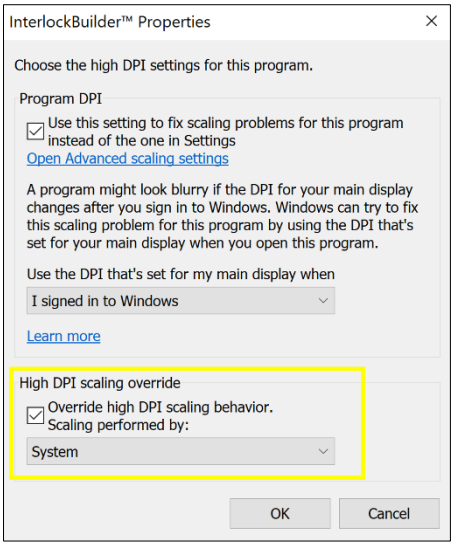


Figure 11 - High DPI Settings

2.7 CREATING AN INTERLOCK BUILDER PROJECT

You should have received a .ILK file that contains information about your hardware. You can use that file to create an Interlock Builder project.

That file supports a range of identical systems to be programmed with one system project file.

1. Open Interlock Builder.
2. From the File menu, choose Open, and navigate to the ILK file.
3. Select it and click Open.
4. If you have schematics or field connect information that you want to use, from the File menu, choose Import.
5. To import schematic files, select Schematic, navigate to the .SCD file you want to use and click Open.
6. To import field connect data, select Field Connect, navigate to the .CSV file you want to use and click Open.
7. From the File menu, click Save As and name your new project file, then click Save.
8. Start drawing schematics, adding labels, and setting properties in your new file.

3 USER INTERFACE TOUR

The main Interlock Builder application window contains:

- Schematics area where interlock logic can be designed using one or more tabbed schematic sheets
- Menu bar and toolbars which provide access to file management, schematic editing & programming, and view control functions
- Dockable panes, including individual views for Interlocks, Properties, Monitor (including Schematic and Field Connect), and Log Output views

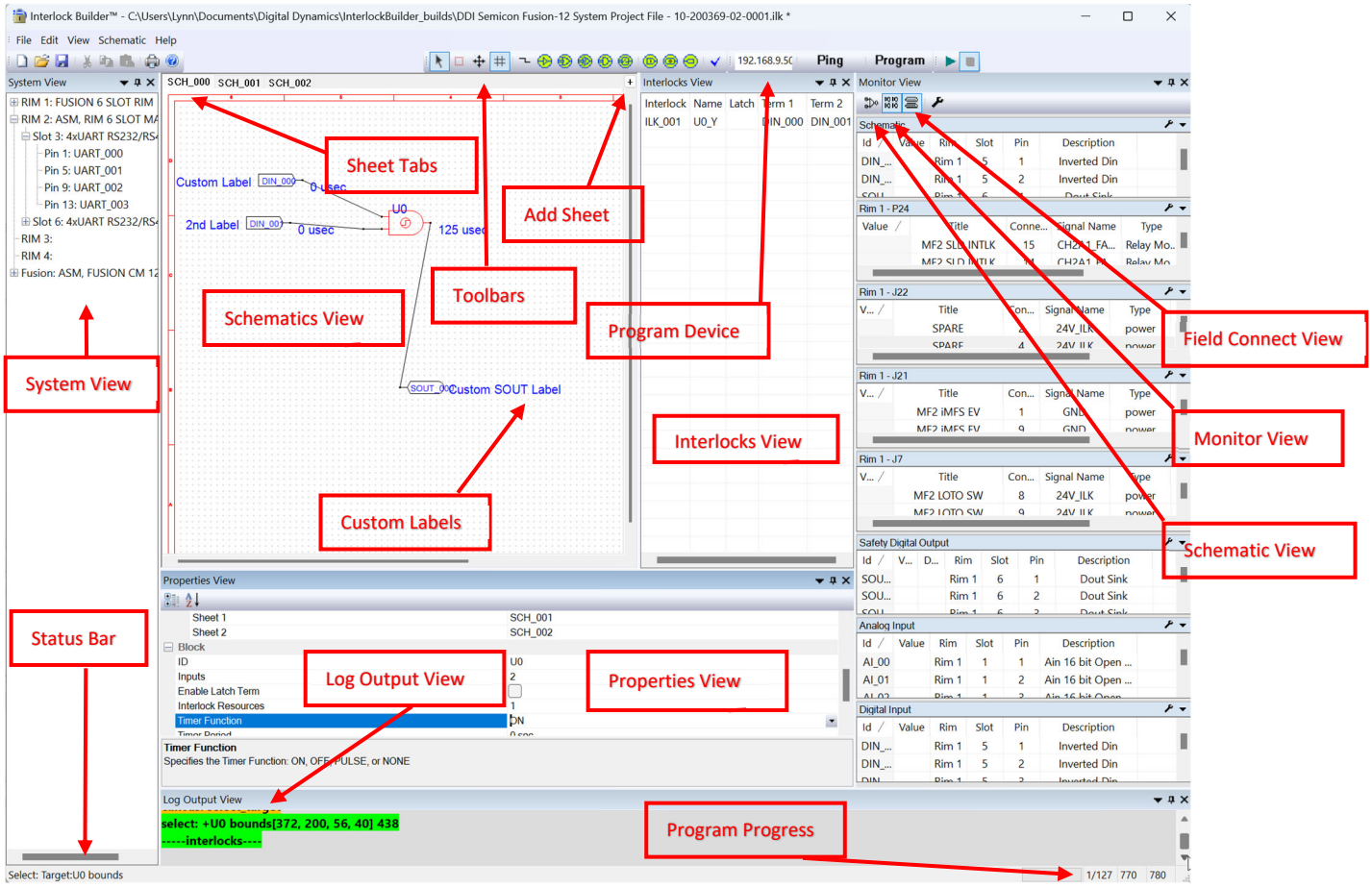


Figure 12 - Main Interlock Builder Window

The Monitor View, Schematic View, and Field Connect View share the same pane. Click the icons to switch the view.

3.1 DOCKABLE VIEWS

The Interlocks View, Properties View, Monitor and Field Connect Views, and Log Output View are dockable panes which can be repositioned at the left, right, top, or bottom of the main window. They can also be set as floating windows or grouped together in a tabable pane. Use the View menu to open any panes not currrently open.

Dragging a view title bar shows the dockable sites where it can be relocated.

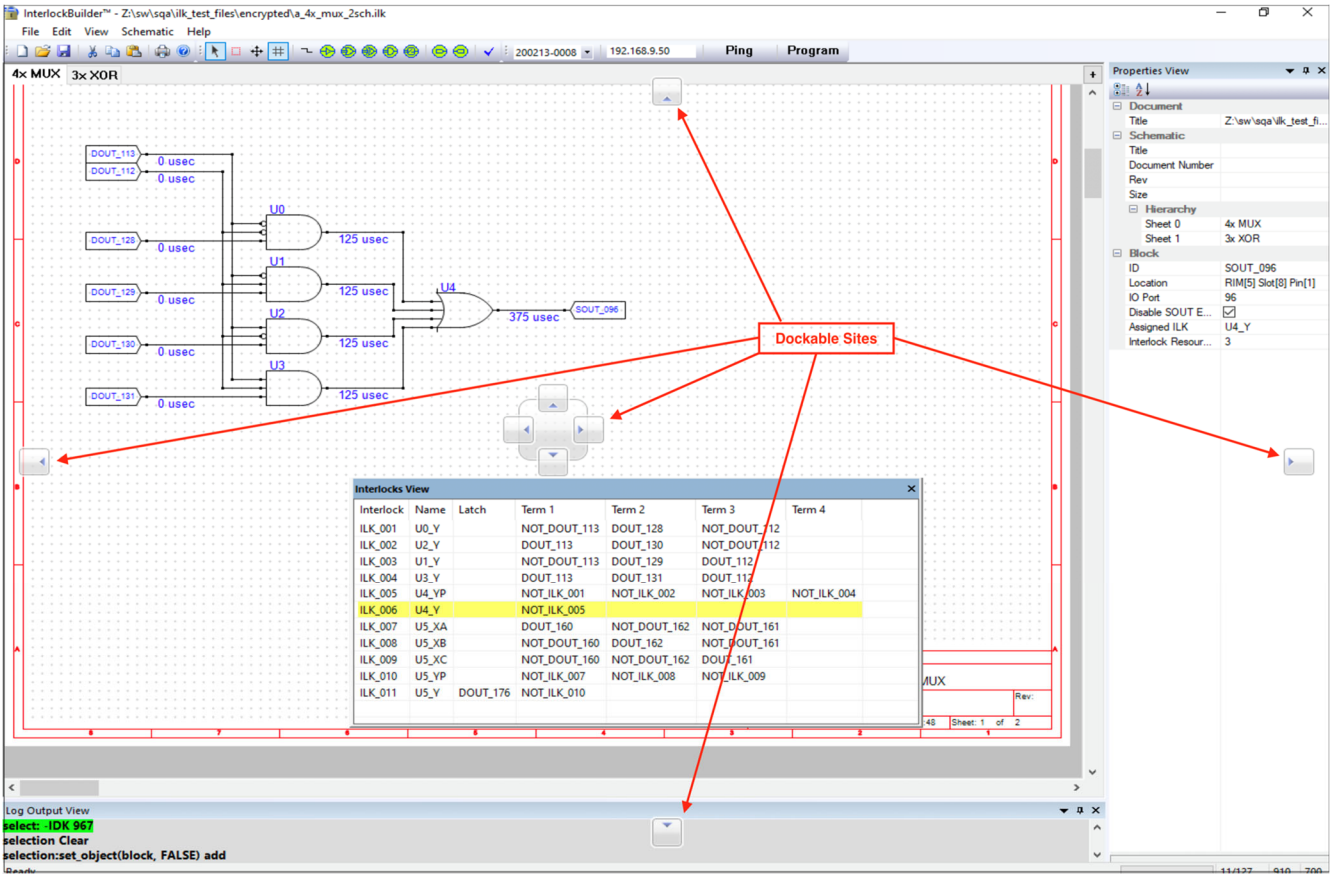


Figure 13 - Docking Sites

Panes can be grouped together in docking sites or arranged as tabbed panes.

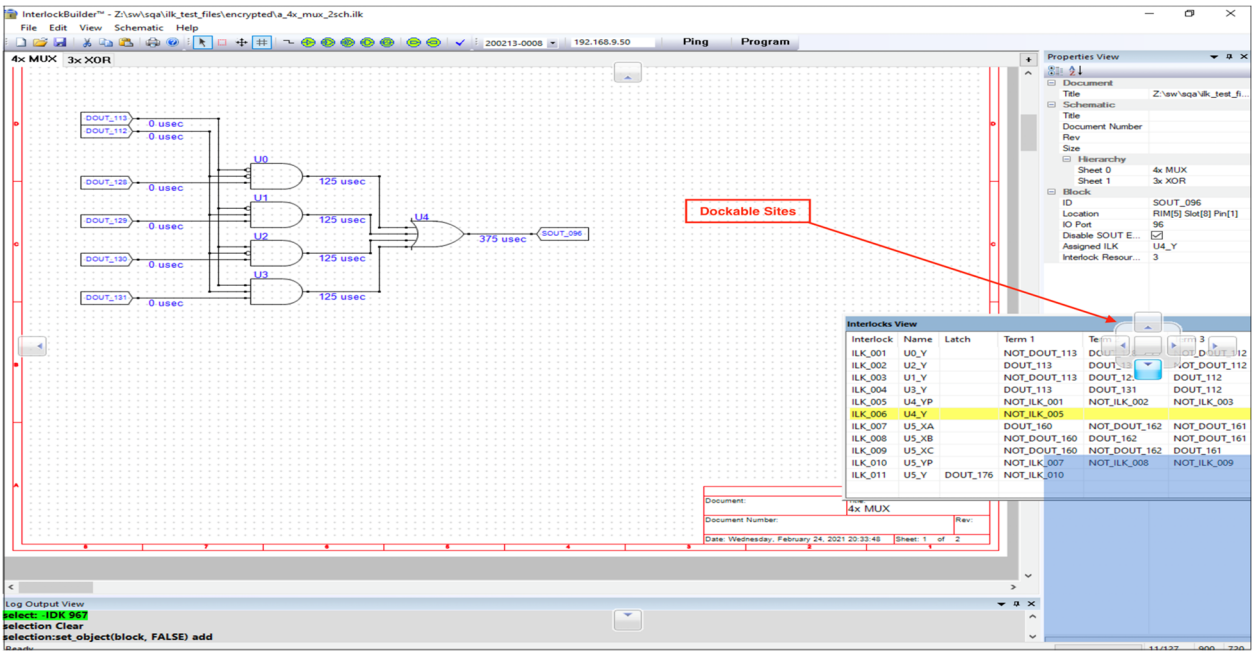


Figure 14 - Docking Sites (grouped)

Click the arrow located in the title bar of any pane to show options to Float, Dock and Auto Hide.

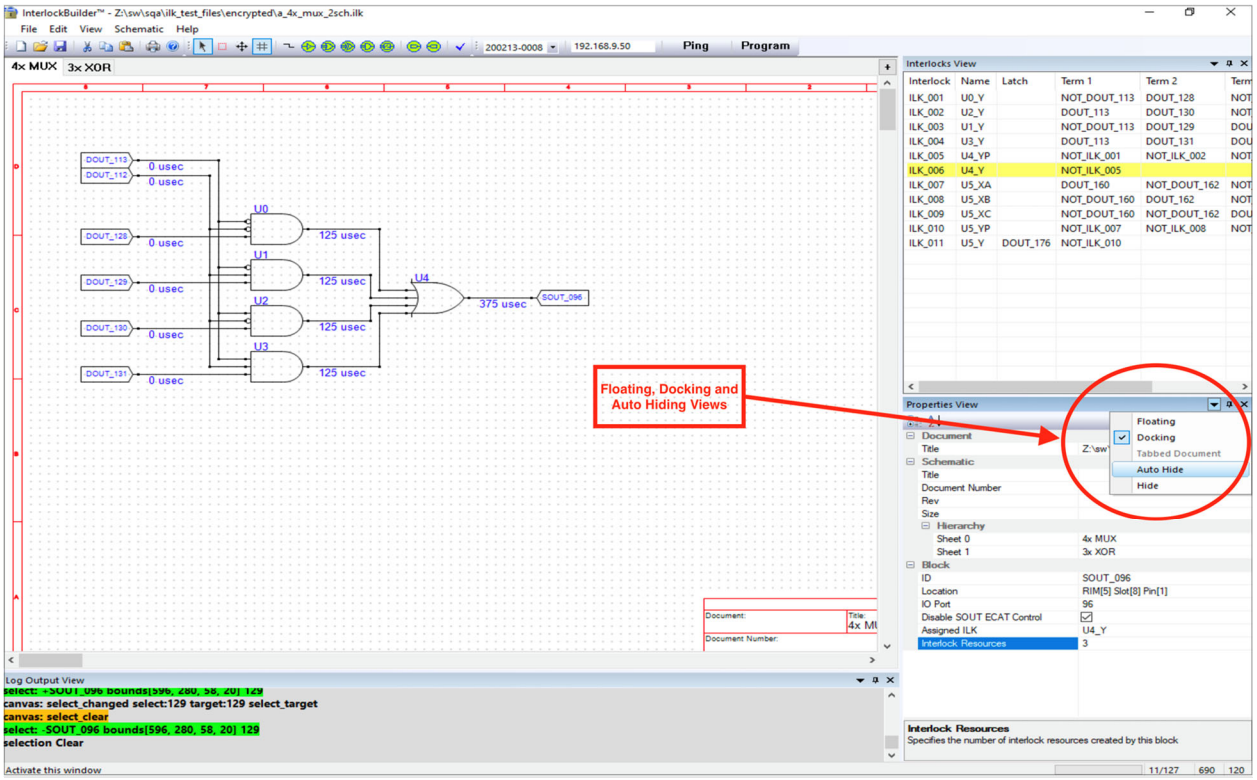


Figure 15 - Floating, Docking and Auto Hide

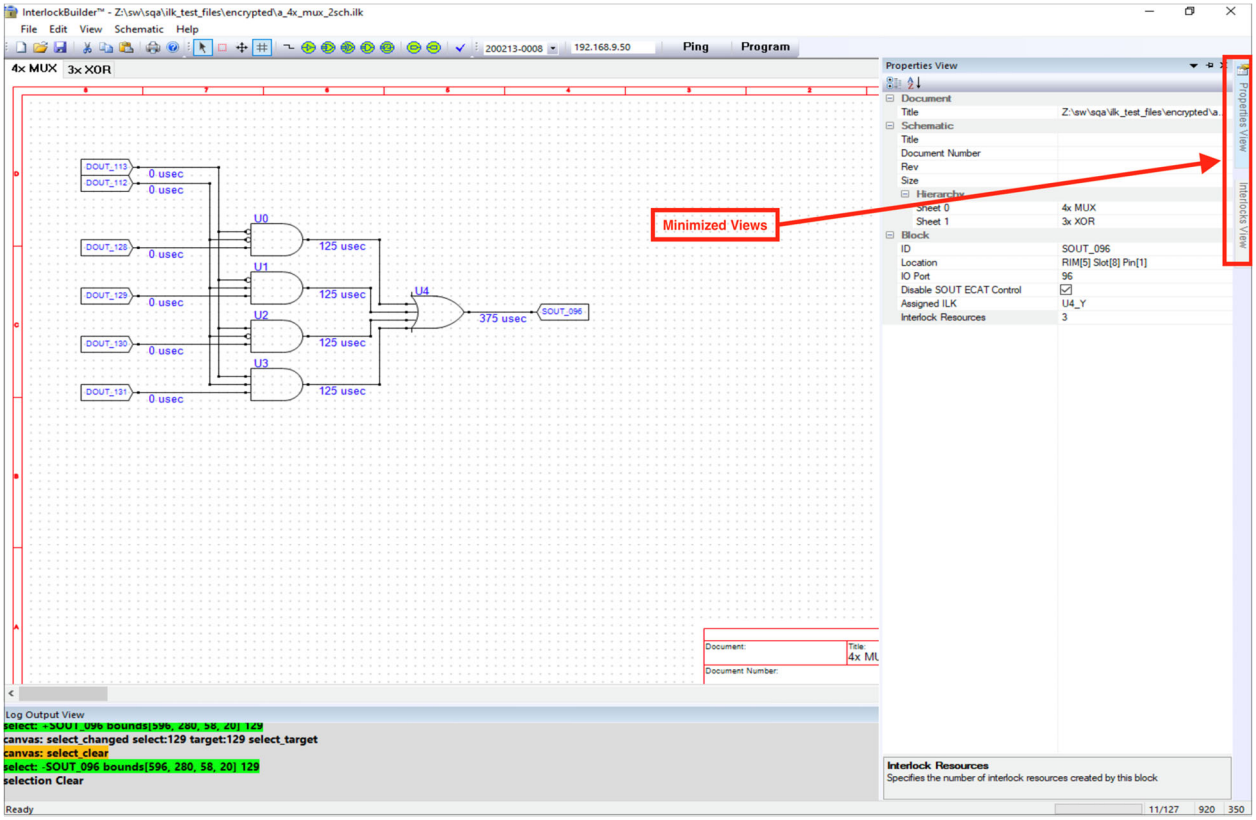


Figure 16 - Hidden Views

3.2 SCHEMATIC VIEW

You can add sheets, rearrange the sheet order, and delete schematic sheets.

To add a new schematic sheet, click the plus button to the right of the schematic pane.

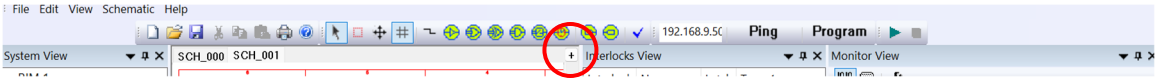


Figure 17 – Add Schematic tab

To import schematic sheets, from the File menu, select Import > Schematic. Navigate to the schematic file, select it, and click Open.

To change the order of the tabs, from the Schematic menu, click Order Schematic Tabs and in the dialog box, use the arrows to change the order., and click OK.

To delete a schematic sheet, right-click the sheet tab name and click Yes to confirm the deletion.

3.3 SYSTEM VIEW

The System View lists all of the RIMs, slots, and channel IDs in order. You can use this view to reference which channel ID goes to which RIM Slot Pin when determining which IO Port number you want to use within your schematic.

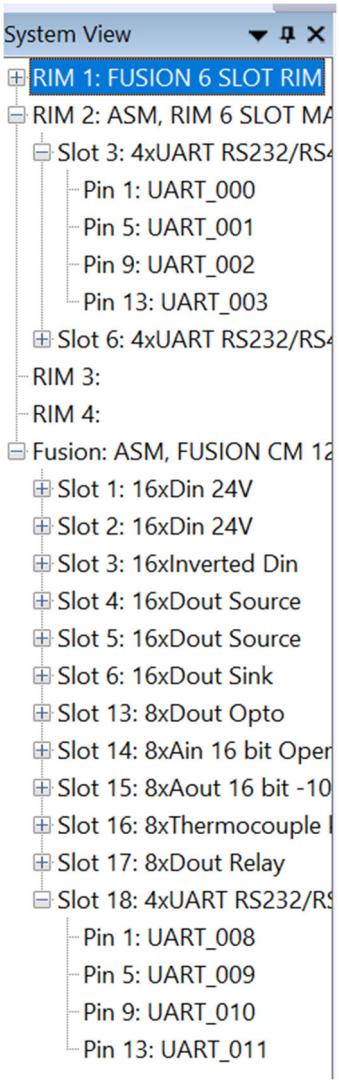


Figure 18 System View

3.4 INTERLOCKS VIEW

The Interlocks View shows details of the interlocks which have been designed in Interlock Builder.

Each interlock you design consists of one or more interlock resources, which is the unit of allocation. In Figure 19 - Interlocks View, the Interlock column shows the individual interlock resources used in a particular design. Each interlock resource has one or more input terms, and those terms are shorn in the Term 1, Term 2, Term 3, and Term 4 columns in Figure 19 - Interlocks View. A Fusion.IO system has a total of 127 available interlock resources. Note that every gate is

converted into AND gates via DeMorgan's law. This means that some gates may take up more interlock terms than others. To learn more, see https://www.electronics-tutorials.ws/boolean/demorgan.html.

The Latch is shown here too where you'll see the name of the latch. To learn more about latches, see section, 4.6 Latches.

Click any logic gate or input port in the schematic drawing to highlight the interlock resources generated by that object in light gray. Click a SOUT port to highlight the interlock resource assigned to the SOUT in yellow.

Interlocks View

Interlock	Name	Latch	Term 1	Term 2	Term 3	Term 4
ILK_001	U0_Y		NOT_DOUT_113	DOUT_128	NOT_DOUT_112	
ILK_002	U2_Y		DOUT_113	DOUT_130	NOT_DOUT_112	
ILK_003	U1_Y		NOT_DOUT_113	DOUT_129	DOUT_112	
ILK_004	U3_Y		DOUT_113	DOUT_131	DOUT_112	
ILK_005	U4_YP		NOT_ILK_001	NOT_ILK_002	NOT_ILK_003	NOT_ILK_004
ILK_006	U4_Y		NOT_ILK_005			
ILK_007	U5_XA		DOUT_160	NOT_DOUT_162	NOT_DOUT_161	
ILK_008	U5_XB		NOT_DOUT_160	DOUT_162	NOT_DOUT_161	
ILK_009	U5_XC		NOT_DOUT_160	NOT_DOUT_162	DOUT_161	
ILK_010	U5_YP		NOT_ILK_007	NOT_ILK_008	NOT_ILK_009	
ILK_011	U5_Y	DOUT_176	NOT_ILK_010			

Figure 19 - Interlocks View

The Interlocks View is updated whenever any change is made to the schematics drawing, and the total number of used and available interlock resources are shown in the status bar.

Figure 20 - Interlocks Status Bar (used/available)

3.5 MONITOR VIEW

The Monitor View is a dockable pane in Interlock Builder which displays the status of input and output channels present in a connected Fusion.IO system and allows you to filter which channels are displayed according to the channel type and slot card location. You can also view schematic, or field connect information as described later in this document. If field connects are imported, the Field Connect view is the default view, otherwise the Schematic view is the default.

Schematic, I/O Monitor, and Field Connect icons

Figure 21 - Monitor View Toolbar Icons

I/O channels are grouped in the Monitor View by general types:

- **Safety Digital Output (SOUT) -** A safety digital output (SOUT) is a digital output channel which can be controlled by a programmed interlock as well as by an EtherCAT master.
- **Digital Input (DIN) –** A digital input channel which can be used as an input term to an interlock.
- **Analog Input (AIN) –** An analog input style channel which can include -10…+10V, 4-20mA, thermocouple, and RTD signals. Analog inputs are not available to be used in Interlocks.
- **Analog Output (AOUT) –** An analog output style channel, for example -10..10V and 4-20mA outputs. Analog outputs are not available for use in interlocks.

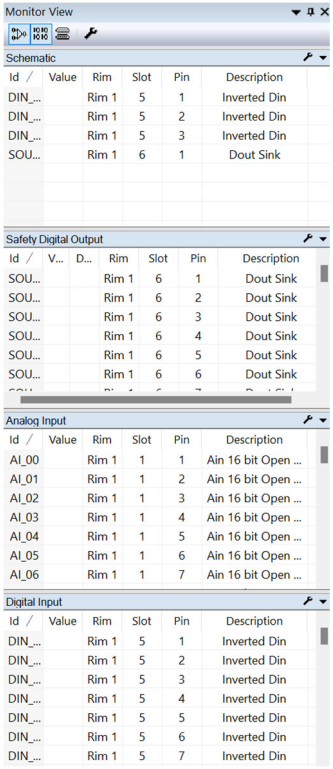


Figure 22 - Monitor View

Monitor panes show the following details for each I/O channel:

Detail	Description
Id	Logical ID of the I/O used by Interlock Builder to assign I/O channels to interlocks
Value	Value of the associated I/O channel 1) Digital I/O channels: 1 or 0 2) Analog Channels: Physical value (e.g Voltage, Temperature, etc.) or raw (digital) value
RIM	Fusion or RIM device in which this I/O channel is located
Slot	Slot number in which this I/O channel's slot card is located
Pin	Slot card pin used by this I/O channel
Description	Specific type of I/O channel (e.g. sourcing or sinking digital output, inverting or non-inverting digital input, etc.)

Table 1 - Monitor View Details

Each Monitor pane also has two controls in the upper right corner which can be used to expand or collapse the pane and to set properties such as display filters and format of the channel data.

Control		Description
Expand/Collapse		When the arrow is pointed down you can click to collapse the pane. To expand the pane, click the arrow pointing to the right.
Properties		Opens a properties dialog, which is specific to each Monitor pane.

Set Display filters using the Monitor properties to control which I/O channels are shown in Monitor view based on:

- Fusion or RIM device where the I/O channel is located
- Slot card on which the channel is located
- Specific type of I/O channel

You can reduce the number of IO channels that are displayed, by removing selected values, which is useful when your system has many IO channels. Select OK to apply the filter.

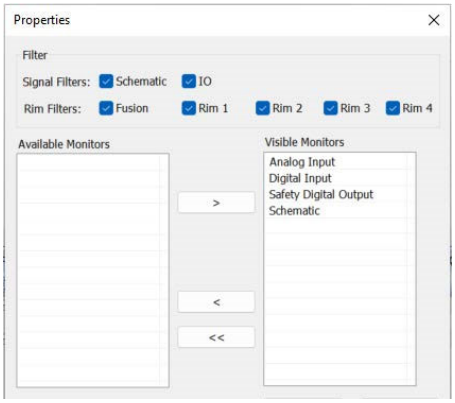


Figure 23 - Monitor Display Filters

Use the Analog Input and Analog Output Monitor panes to set whether the channel data value is displayed as a physical (e.g. voltage) or as a raw value. The numerical format for raw values can be set to either decimal or hexadecimal value.

Click the Filter tab of the Monitor Properties and click the checkbox to hide non-Input /Output for that channel depending on your need.

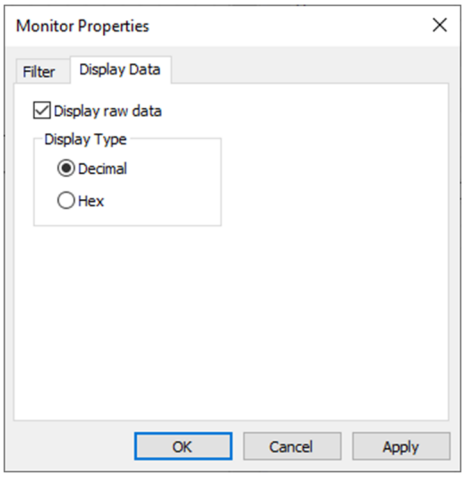


Figure 24 - Monitor Data Format

Hover the cursor over an I/P port to view the block's rim, slot, and pin information.

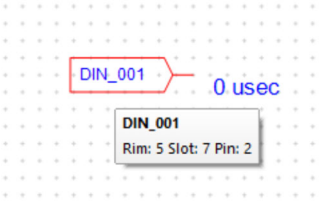


Figure 25 - Help Hint

3.6 SCHEMATIC MONITOR VIEW

Displays a streamlined representation of the Digital IOs' seen on a schematic sheet. This works the same as the IO Monitor, except that only the IO's in the current schematic tab are shown. Figure 26 - Schematic Monitor View shows a schematic monitor view representing the current schematic IOs.

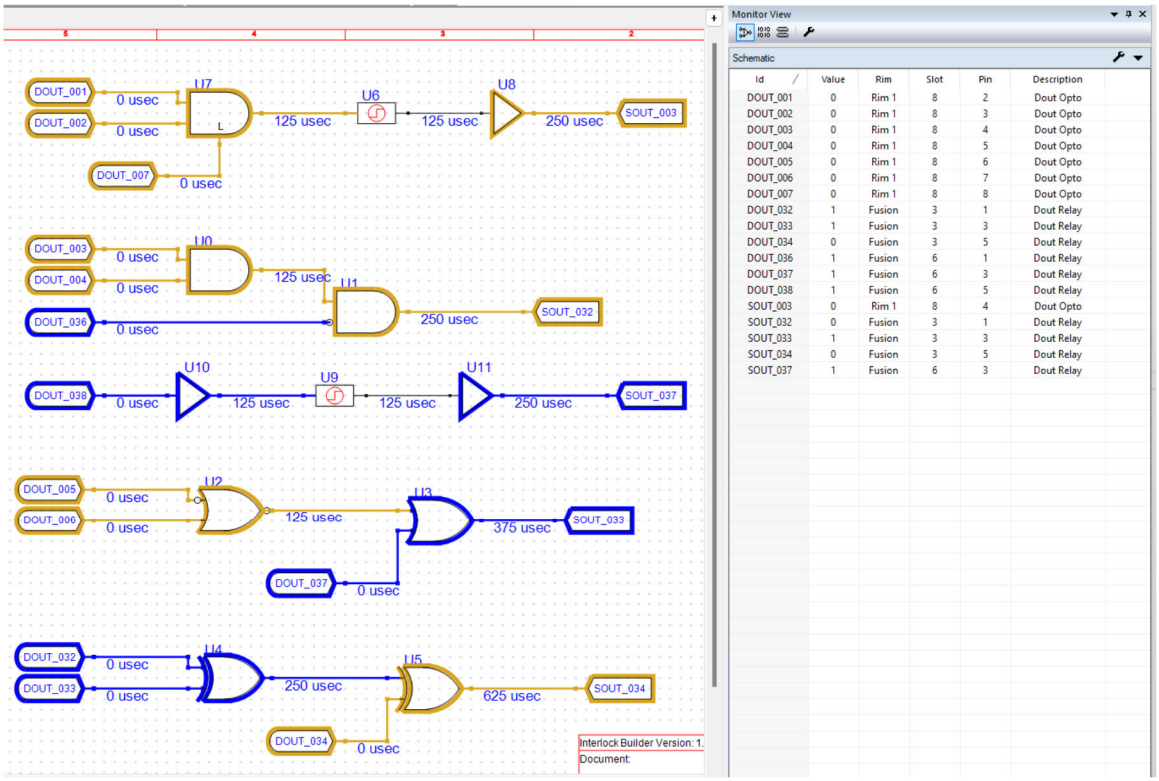


Figure 26 - Schematic Monitor View

3.6.1 Live Monitor Schematic Indicators

Live monitoring of I/O includes bold highlights around each I/O block, logic gate, and wire in the schematic while the live monitor is being run. A yellow highlight indicates the signal is low and a blue highlight indicates the signal is high.

To enable this mode, connect to the appropriate unit via LAN, open the system project file, and press the live I/O Monitor button within Interlock Builder. This live I/O data updates at a rate of 1Hz.

Figure 27 - Live I/O Monitor Button

IO Port Blocks on the schematic show the appropriate state for the signal given the specifications in the block's Properties View, regardless of the schematic loaded. This data is also mirrored within the Monitor View pane.

Intermediate logic gates and wires, however, are tied specifically to the interlock schematic loaded onto the Fusion.IO device. If the schematic's interlock terms change from what is currently loaded on the Fusion.IO unit, these highlighted signals may be indicative of the actual states of the logical gates. Live first-class timer IO states are not shown on the schematic. Instead, the gate that appears directly before the first-class timer takes the timer's functionality into account

when displaying the live state. For example, if an AND gate fed into a 1 sec ON timer, the AND gate itself is not shown high until it is fed a rising edge and a second has passed to satisfy the timer.

3.7 FIELD CONNECT VIEW

Once you import field connect data, you can view it in Interlock Builder. Field connect data is stored in a CSV file format.

To import field connect data:

1. From the File menu, select Import > Field Connect.
2. Navigate to where the field connect file is located, select the file, and click Open.
3. Click the icons at the top of the Monitor view to change between the Schematic, Monitor, and the Field Connect views.

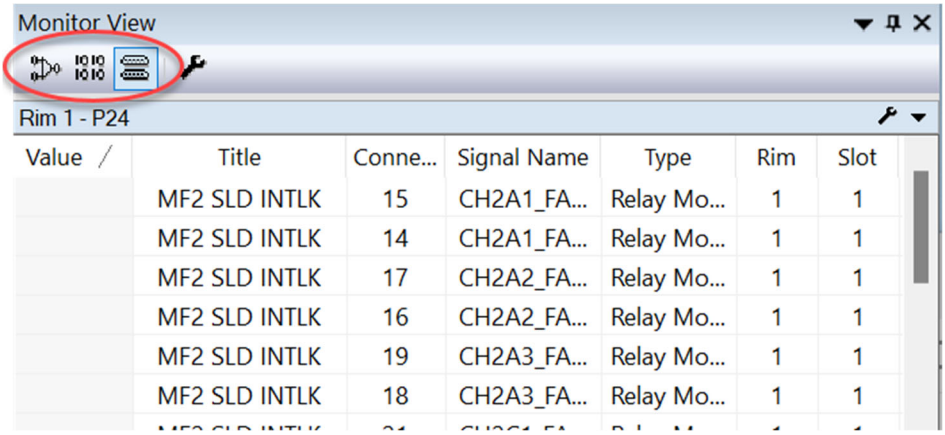


Figure 28 – Field Connect view

Each of the RIMs are listed in the Monitor view window although only one is shown in this figure.

You can view the Connector Pin, Signal Name GND, Type power, RIM, Slot, and Pin details.

3.8 PROPERTIES VIEW

The Properties View shows information about interlock objects (e.g. logic gates, IO Ports, etc.), schematic sheets, and the project document, including several properties which can be customized.

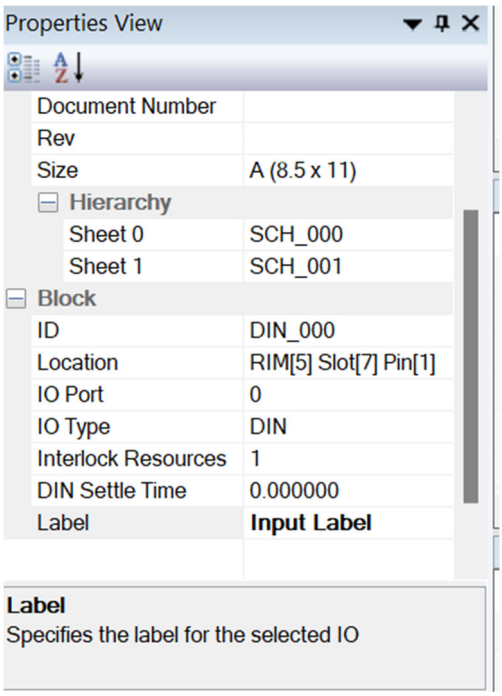


Figure 29 - Properties View

3.8.1 Block Properties

Click any I/O port or logic block to show the properties for that object as shown in Table 2 - Properties of Schematic Blocks.

Property	Purpose	Editable	Used By
ID	Logical ID of the block (e.g. U2, DIN_001)	no	All objects
Location	Specifies the RIM, Slot and Pin location of the IO port	no	All I/O Ports
IO Port	Specifies the physical I/O used by an I/O port	yes	All I/O Ports
IO Type	Selects if an input port is a DIN or DOUT	no	DIN/DOUT I/O Ports
Interlock Resources	The number of resources allocated by the object	no	All I/O ports & Blocks
DIN Settle Times	The amount of time given for the DIN signal to reach a steady state after changing and can be up to 0.063875 seconds.		DIN Blocks
Disable SOUT ECAT Control	Disable or Enable control of an the SOUT port via EtherCAT	yes	SOUT I/O Ports
Inputs	Sets the number of inputs used by a logic block	yes	Logic Blocks
Enable Latch Term	Enables and shows the interlock latch pin	yes	Logic Blocks
Timer Function	Enables embedded timers in logic gates: Type of timer block to use (e.g. ON, OFF, etc.)	yes	
Timer Period	Time interval used by a timer block	Yes	Intermediate Logic Gates
Label	Identifies the block.	Yes	All I/O Ports

Table 2 - Properties of Schematic Blocks

SOUT and DOUT

DOUTs are digital outputs that you can use as input terms for interlocks by dragging them from the toolbar. By default, the SOUT and corresponding DOUT are not paired together. Check the "Enable paired ECAT Control“ property checkbox to enable the DOUT control. When unchecked, it ignores the ECAT values set via the inherent hidden AND gate.

The paired SOUT and DOUT IO Ports always match. ECAT control can still affect the final SOUT if it is added manually to the schematic via a DOUT IO Port.

Notes

You must click the “Disable SOUT ECAT Control” property checkbox if an interlock’s SOUT does not require control via EtherCAT.
Changing the number of inputs for a block with signals detaches any signals from the input pins that were removed.

3.9 LOG OUTPUT VIEW

Right-click in the Log Output View and select an option to copy, paste, or clear the log output view.

3.10 SCHEMATIC PROPERTIES

The title block properties for schematic sheets can be edited in the Properties view, including:

- Main Document Title
- Document Number
- Sheet Title
- Revision

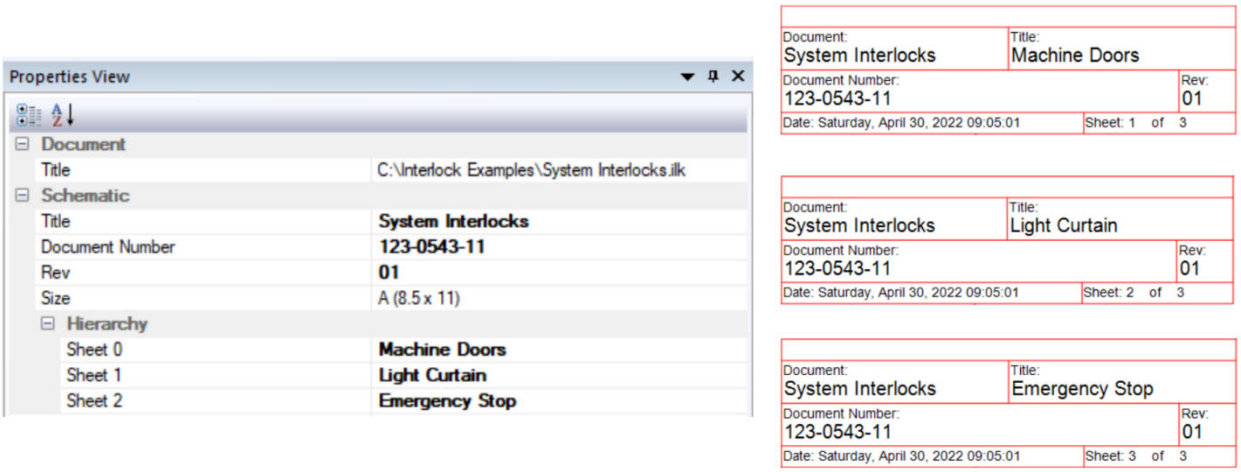


Figure 30 - Schematic Document Properties

To change the text that displays in the schematic sheet, from the Schematic menu, choose Document Titles. In the dialog box, you can edit the names that display. For example, you can change the Document Number to Document Revision Number.

3.10.1 Adding and Importing Labels

You can add labels as you create I/O ports, or you can import existing field connect signal names to block labels in the schematic. You must have imported a field connect file before you can import the labels.

To add labels to the schematic, select the I/O port you want to label and in the Properties view, scroll down and click Label then type the label you want to use. Note this is only for I/O ports and does not apply to intermediate logic gates (like AND gates).

To import labels, from the Schematic menu, choose Import Labels. Specify the settings you want to use and click Import. You can import labels for all tabs or the current tab, while the Overwrite setting specifies whether existing labels get overwritten.

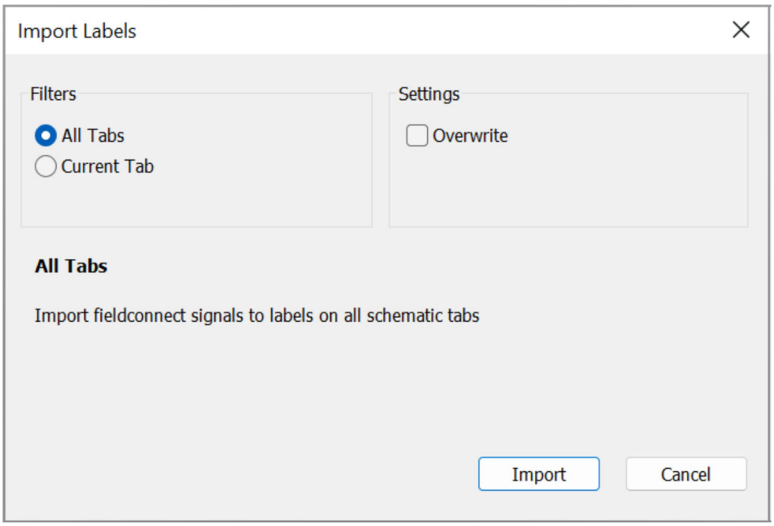


Figure 31 - Import Labels Dialog Box

3.10.2 Import label default behavior

You can specify to always import label names statically or dynamically. The static option is the default setting and does not update label names when a new block is added, a block's port number is altered, or a block's type is changed. When you specify dynamic, Interlock Builder automatically updates label names upon addition of a block, or changes in a block's port number or IO type.

From the Schematic menu, choose Properties. Select Static or Dynamic and click Apply.

3.11 TOOLBARS

3.11.1 Standard Toolbar

The Standard Toolbar provides file and edit functions such as:

- **Create, Open, & Save** schematic documents
- **Cut, Copy, & Paste** clipboard selections
- **Print** schematic document
- **Help** in Interlock Builder

Figure 32 - Standard Toolbar

3.11.2 Schematics Toolbar

The Schematics Toolbar provides quick access to editing tools as well as schematic objects such as IO Ports and Logic Gates.

- **Edit, Select, Move, Snap to Grid**
- **Draw Wire**
- **Logic Gates** (Buffer, OR, XOR, AND, Armed Latch)
- **IO Ports** (DIN/DOUT input port and SOUT output port)
- **Design Rules Check (DRC)**

Figure 33 - Schematics Toolbar

3.11.3 Program Toolbar

The Program Toolbar provides functions for programming a Fusion or Control Module (CM).

- **IP Address:** Ethernet IP address of device
- (default is 192.168.9.50)
- **Ping:** check the Ethernet connection
- **Program:** Program interlocks into device

Figure 34 - Program Toolbar

3.11.4 Monitor Toolbar

The Monitor Toolbar provides controls to start and stop the monitoring of I/O channels in your system.

- Press the Play button to start the monitoring
- Press the stop button to stop monitoring

Figure 35 - Monitor Toolbar

Note: You can use the Monitor Properties Field Connect Filter to hide or show certain IO channels depending on your need.

4 DESIGNING INTERLOCKS

Interlock Builder is a schematic design environment where users can quickly and easily define TÜV certified safety interlocks which are programmed into their Fusion I/O controller. These interlocks can combine digital inputs and outputs distributed among connected Fusion and RIM devices and can include logical objects such as:

- **IO Ports**
- **Logic Gates:** AND, OR, XOR, and Buffer
- **Timers:** ON, OFF, and Pulse
- **Latches**

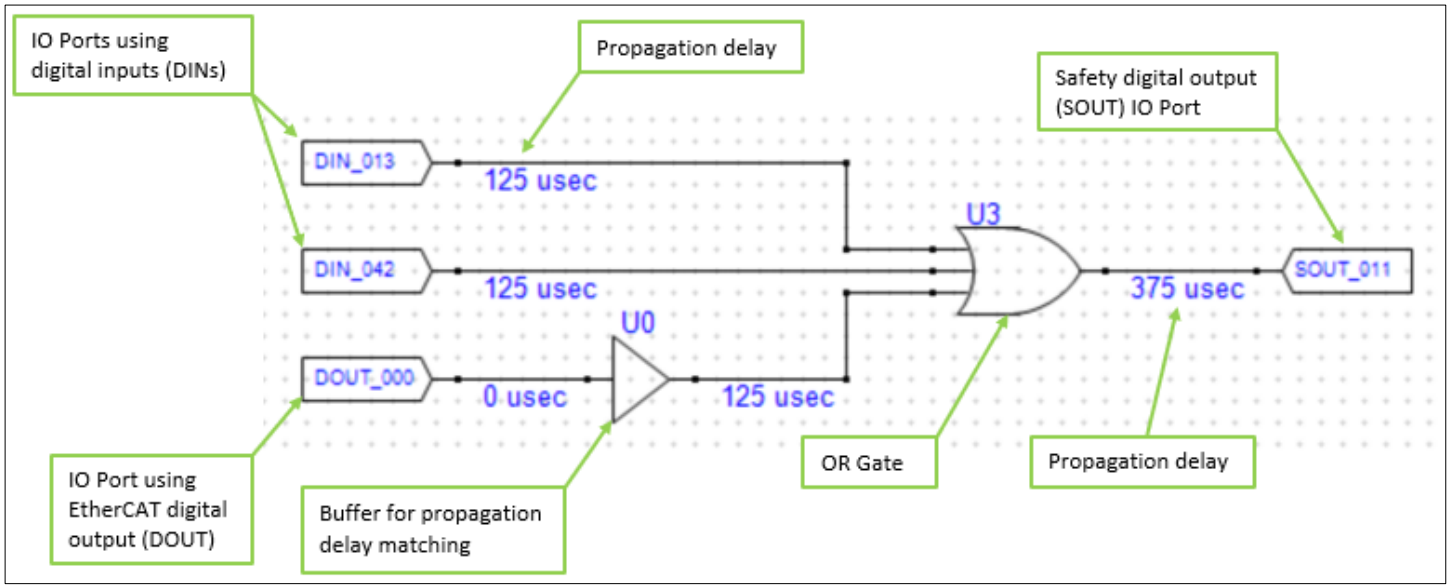


Figure 36 -- Interlock Example

4.1 INTERLOCK TUTORIAL

Let's create a simple interlock to see how this all works. We will create an interlock and test that it works as designed.

This interlock sets a safe digital output (SOUT) when two digital inputs (DINs) are both TRUE. The following blocks are used in this example:

- (2) DIN Ports
- (1) SOUT Port
- (1) AND Gate

To create an interlock:

1) Place and arrange the required blocks as shown in Figure 37 -Blocks Placed & Arranged. Sections 5.1-5.3 provide further detail on placing, selecting, and moving blocks.

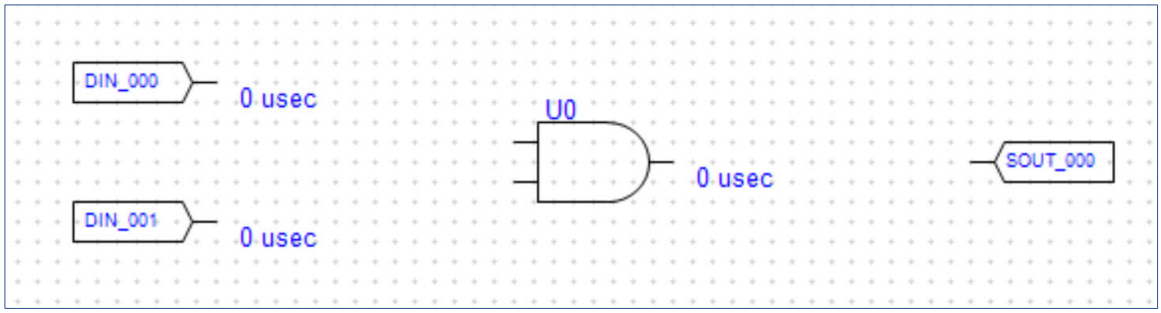


Figure 37 -Blocks Placed & Arranged

2) Change the IO Port properties of each DIN and SOUT port by clicking each IO Port block (Figure 38 - Properties of Selected DIN Port) then changing its IO Port property (Figure 39 - DIN Port Reassigned to IO Port 2). Use the System View to reference which channel ID goes to which RIM Slot Pin when determining which IO Port number you want to use within your schematic. IO Port numbers to use for this example are described here:
   - Assign one DIN port to IO Port 2; the name automatically changes to "DIN_002" after the IO Port property is changed.
   - Assign the other DIN port to IO Port 3 and its name automatically is updated to "DIN_003".
   - The SOUT port is assigned to IO port 0; its name becomes "SOUT_000".

   Note: *Other IO Port values can be used as needed, especially if that is more convenient with your Fusion.IO system hardware.*

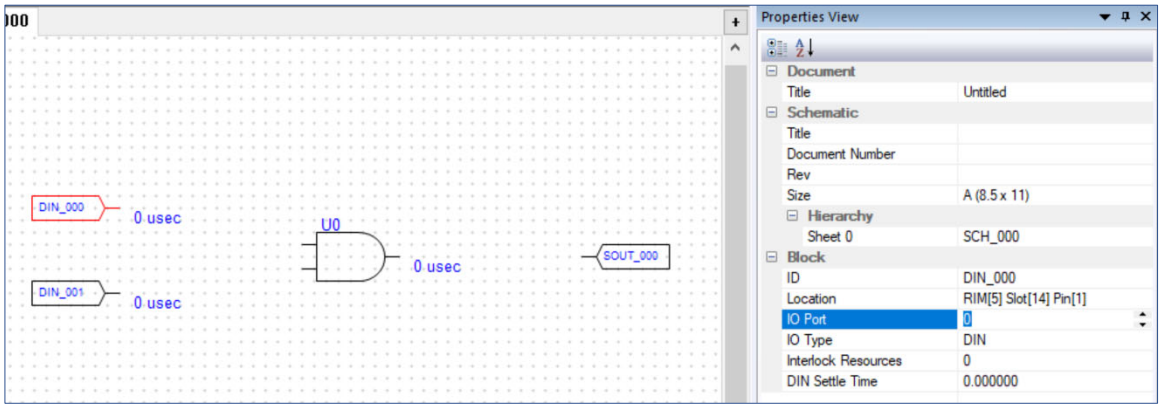


Figure 38 - Properties of Selected DIN Port

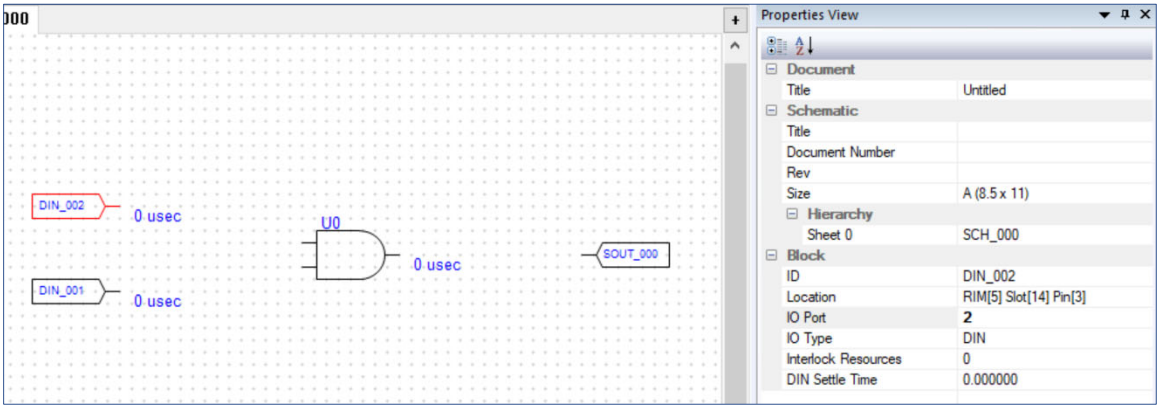


Figure 39 - DIN Port Reassigned to IO Port 2

3) For initial testing disable the "Enable Paired ECAT Control" property of the SOUT port.
   - ***Note**: Leave this property disabled if the final application requires control of this SOUT via EtherCAT. Be sure to re-program the interlocks into the Fusion device after this property is changed.*

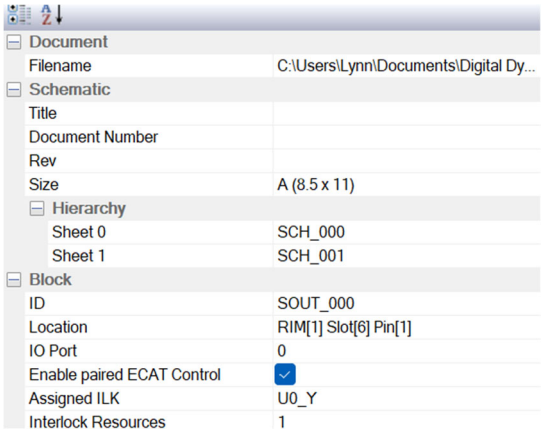


Figure 40 – Enable Paired ECAT Control Property

4) Connect blocks with wires. The section 5.4 Inverting PinsInverting Pins, provides details on how to wire blocks to-

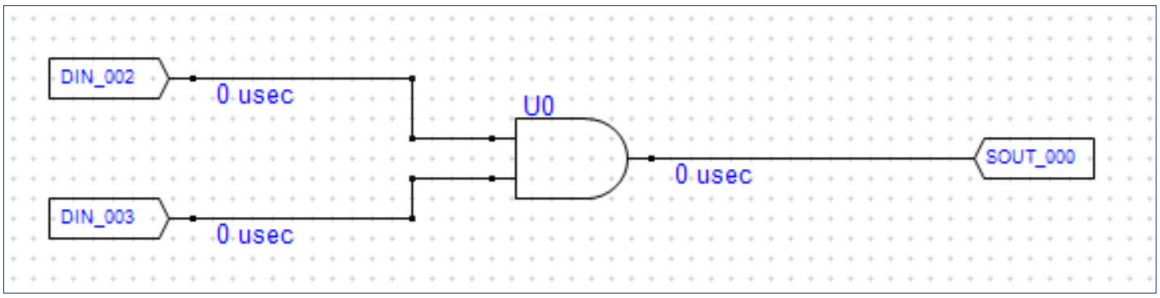


Figure 41 - Blocks Connected with Wires

gether.

5) Click the Design Rules Check (DRC) button to check the schematic for errors, such as missing or incomplete connections.
   - An example of how the DRC indicates a missing connection is shown in Figure 42 - DRC Detects Missing Connection on SOUT Port

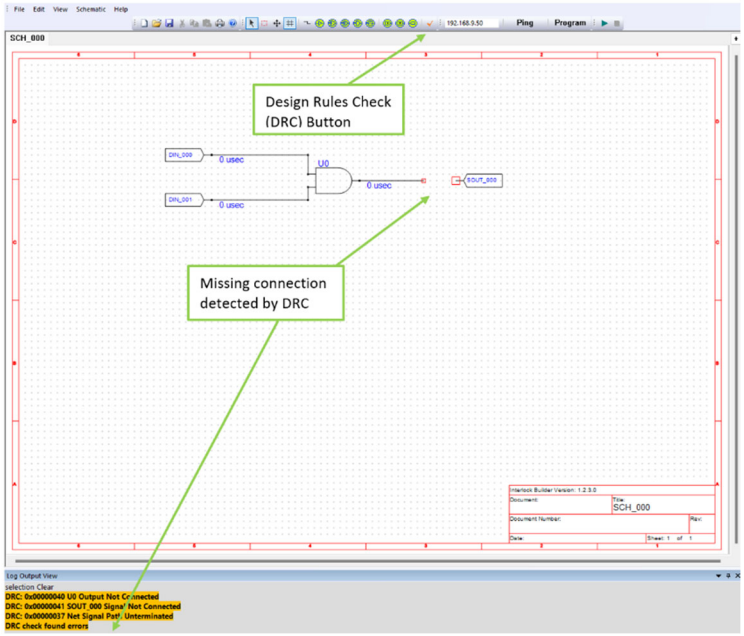


Figure 42 - DRC Detects Missing Connection on SOUT Port

- Figure 43 - DCR Completed Successfully shows a Design Rules Check (DRC) for this example which passed successfully.

- Program Fusion.IO system with interlocks. The chapter PROGRAMMING INTERLOCKS provides details on how to program interlocks into a Fusion device.

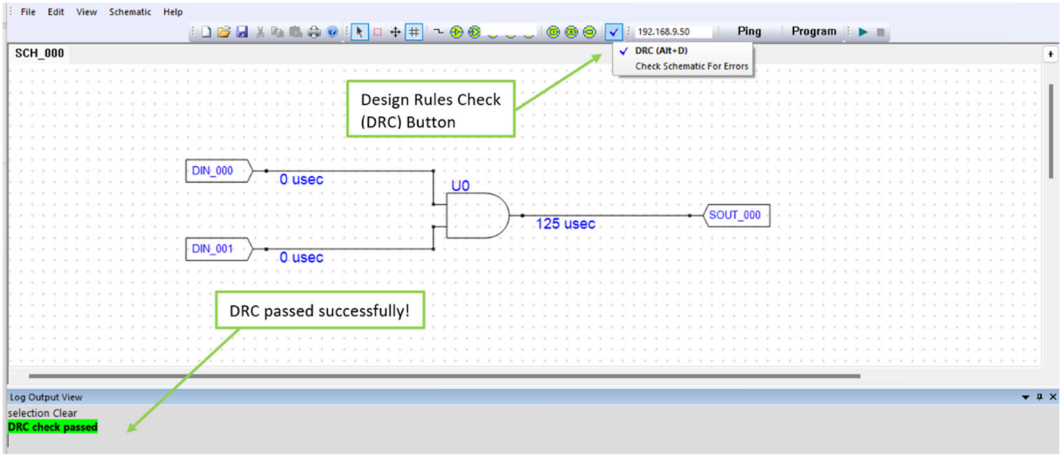


Figure 43 - DCR Completed Successfully

Test the interlock by changing DIN and DOUT states and monitor the results through Monitor View.

***Note**: further details about Monitor View can be found in the section* Monitor View.

a) Test DIN_002 (See Figure 44 - Testing DIN_002).
   i) Click the Play button to start online monitoring of the system's I/O states.
   ii) Activate DIN_002 and verify in Monitor View that it is active (TRUE). A value of 1 in Monitor View means that the input is active.
   iii) Notice that SOUT_000 has a value of 0, which means that it is not active (TRUE). This is because SOUT_000 is controlled by an interlock which is TRUE only when both DIN_002 and DIN_003 are TRUE.

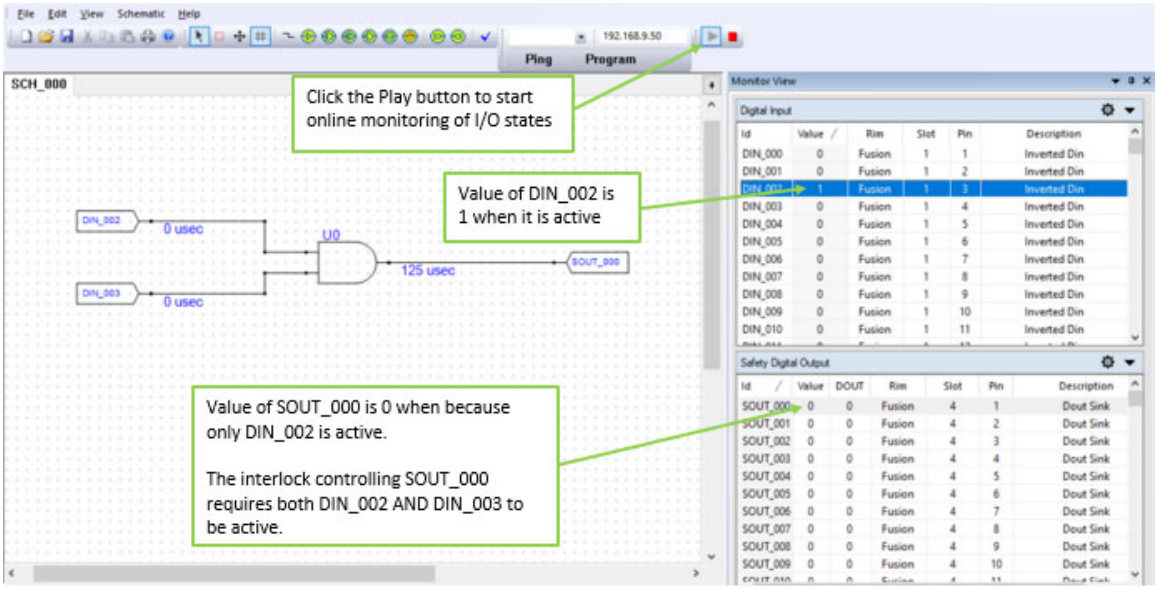


Figure 44 - Testing DIN_002

b) Test with only DIN_003 (See Figure 45 - Testing DIN_003.)
   i) Activate DIN_003 and verify in Monitor View that it is TRUE.
   ii) Notice that SOUT_000 has a value of 0, which means that it is not TRUE. This is because SOUT_000 is controlled by an interlock which is TRUE only when both DIN_002 and DIN_003 are TRUE.

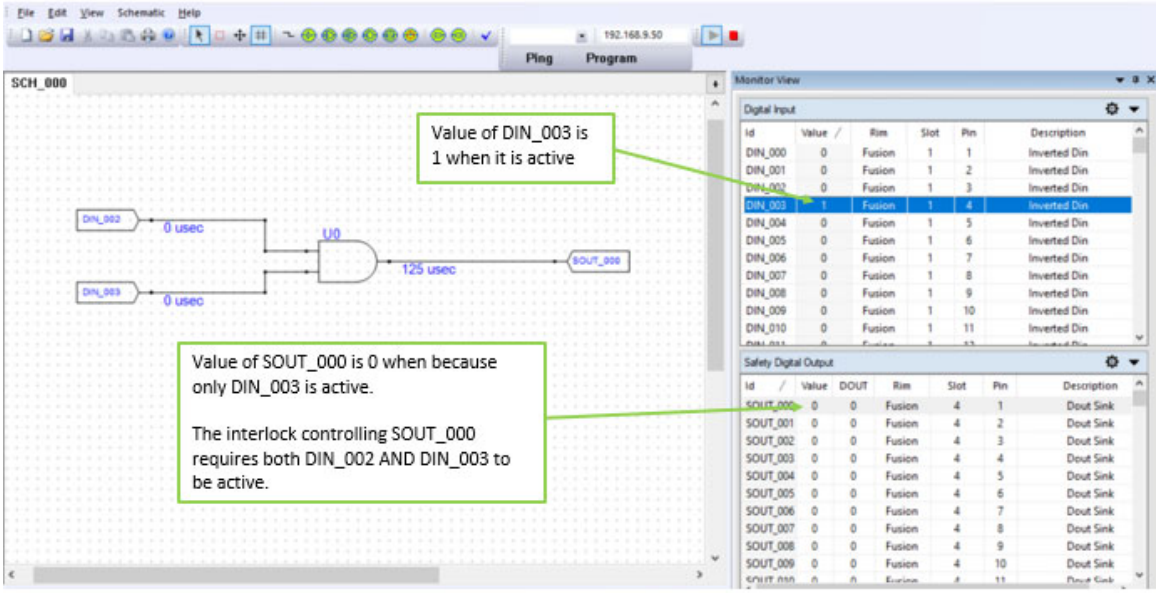


Figure 45 - Testing DIN_003

c) Test with both DIN_002 and DIN_003 (See Figure 46 - Testing DIN_003.)
   i) Activate both DIN_002 and DIN_003 and verify with Monitor View that they are both active (TRUE).
   ii) When both DIN_002 and DIN_003 are TRUE, SOUT_000 will also be TRUE.
   iii) If SOUT_000 is TRUE in this test, then your interlock is working.

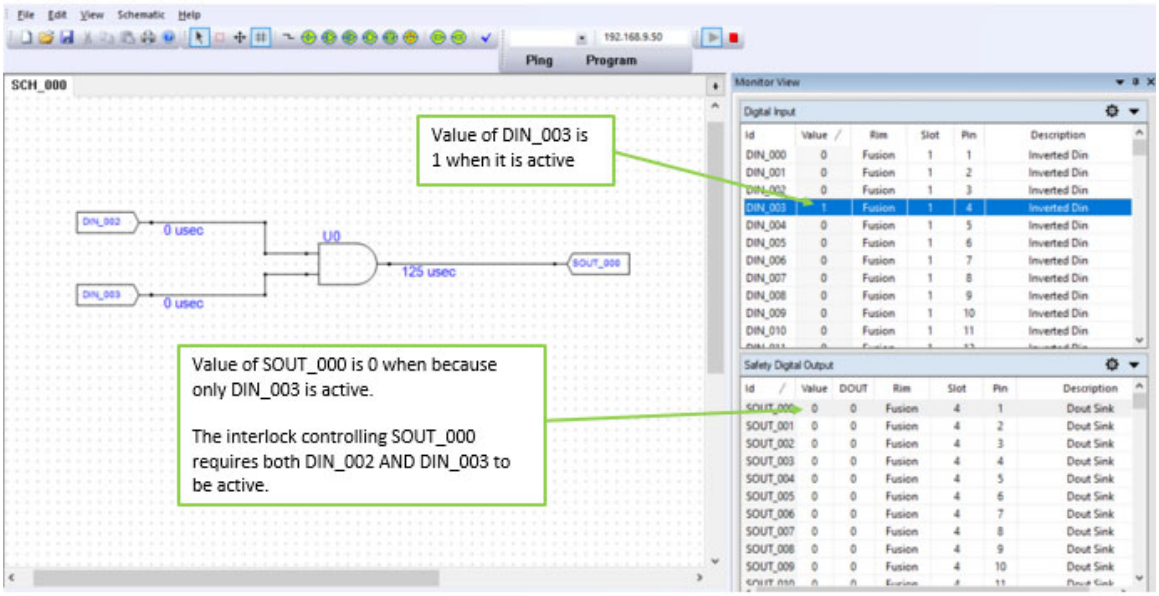


Figure 46 - Testing DIN_003

After you've completed the tutorial, we'll take a closer look at more design elements.

4.2 SCHEMATIC BLOCKS

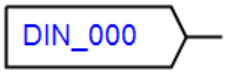
Now, let's look at these schematic blocks and how they are used:

- IO Ports
- Logic Gates
- Timers
- Latches

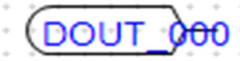
4.3 I/O PORTS

I/O Ports designate the inputs and outputs that are used with an interlock. Each I/O Port has a property, “IO Port” which assigns the port to a physical I/O channel.

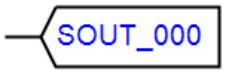
Inputs to interlocks can be either:

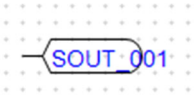
- Digital inputs (DIN) 

- or -

- Digital outputs (DOUT) which are set via EtherCAT 

The type of input used by an I/O Port, DIN or DOUT, is viewed in the Properties View.

Outputs which are set by interlocks are safety digital outputs (SOUT) 

- Looks like this when the Enable paired ECAT Control checkbox is checked: 

SOUT and DOUT

Each SOUT includes a DOUT term which allows the SOUT to be controlled by programmed interlocks as well as via EtherCAT. Effectively the DOUT term acts like an Enable for the SOUT; the actual state of an SOUT’s pin is the value of the interlock ANDed with the DOUT value set via EtherCAT.

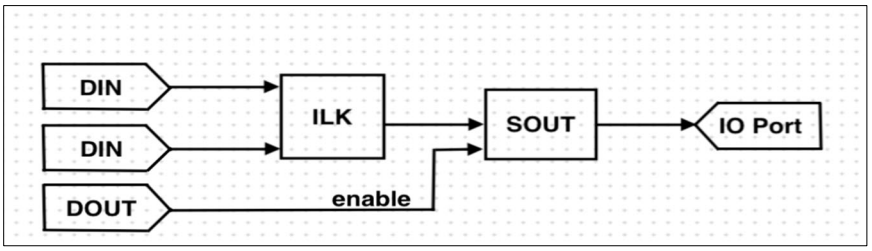


Figure 47 - SOUT and DOUT

Each SOUT I/O Port has a “Enable Paired ECAT control” property which allows an SOUT to enable inherent paired ECAT Control. When this SOUT ECAT control is enabled, an inherent link is created between that SOUT_n and the

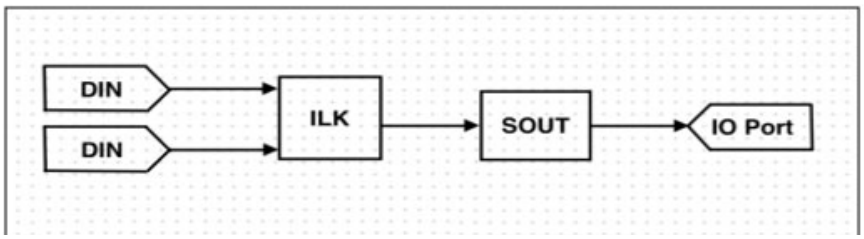


Figure 48 - SOUT with "Disable SOUT ECAT Control" Property Set

corresponding DOUT_n. In this case, the DOUT_n must be asserted, along with the interlock logic being high, for the SOUT channel on the slot-card to be asserted. By default, this property is not set.

When the option for inherent SOUT ECAT control is enabled, the icon for the SOUT IO Port on the schematic updates to visually indicate it is set.

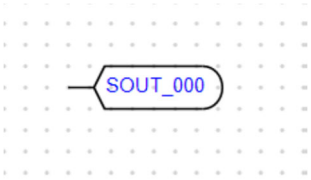


Figure 49 - SOUT with Paired ECAT Control Enabled

When this property is not set, use explicit DOUT gates within the interlock schematic to gain ECAT control.

4.3.1 Adding Labels to I/O Ports

You can add labels to inputs and outputs using the Properties view. Select the input or output and in the Properties view, click Label then type a label for that item. See 3.10.1 Adding and Importing Labels.

4.4 LOGIC GATES

Interlock Builder provides several logic gates which can be used in interlock schematics.

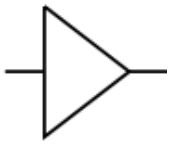
AND, OR, and XOR gates all support up to 32 inputs and provide 2 inputs by default; the number of pins used by a logic gate can be set in the Properties View. Also, input and output pins can be inverted by double-clicking on the pin after the gate is placed in the schematic.

Note: *The graphics and truth tables below show the default two input pins for these logic gates.*

4.4.1 Buffer

The output of a Buffers is:

- TRUE when the input is TRUE
- FALSE when the input is FALSE



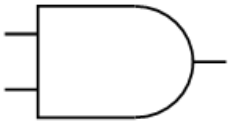
Input	Output
0	0
1	1

A Buffer can be made into a NOT gate by inverting either the input or output.

4.4.2 AND Gate

The output of an AND gate is:

- TRUE when all inputs are TRUE
- FALSE in all other cases

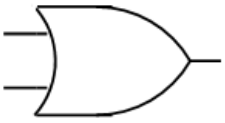


Input 1	Input 2	Output
0	0	0
0	1	0
1	0	0
1	1	1

4.4.3 OR Gate

The output of an OR gate is:

- TRUE when 1 or more inputs are TRUE
- FALSE when all inputs are FALSE

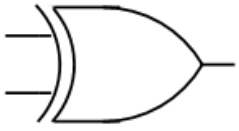


Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1

4.4.4 XOR Gate

The output of a XOR (exclusive OR) gate is:

- TRUE when 1 input is TRUE
- FALSE when all inputs are FALSE or multiple inputs are TRUE



Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	0

4.5 TIMERS

Use timer functions to define timing behaviors within interlocks, for example, adding delays after an input or other interlock signal changes state. Timers can be used with input IO Ports (e.g. DIN or DOUT ports) as well as the outputs of logic gates, other timers, and latches.

Timers are now embedded in logic gates and timer checking is part of the DRC check. You need to add a logic gate after the timer and the DRC check informs you if it is missing. Legacy projects may need logic gates added before and after the timer depending on how they are constructed.

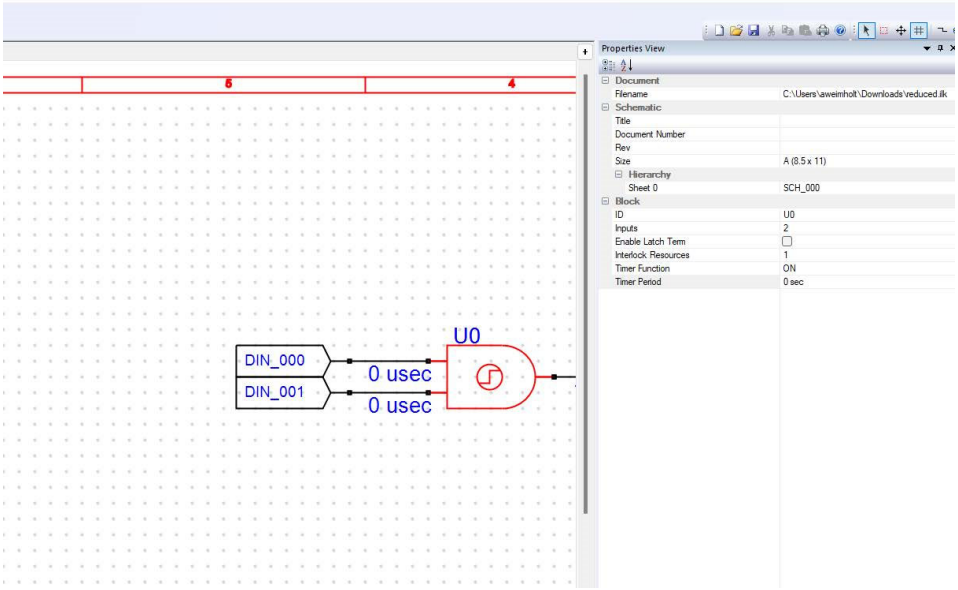


Figure 50 - Embedded Timer

4.5.1 Overview of Timer Functions

The available Timer functions are:

- **ON:** Output set TRUE a fixed time after a rising edge on the input
- **OFF:** Output set FALSE a fixed time after a falling edge on the input
- **PULSE:** Output Produces a fixed time duration pulse after a rising edge on the input
- **NONE**: Disables the timer function; the output

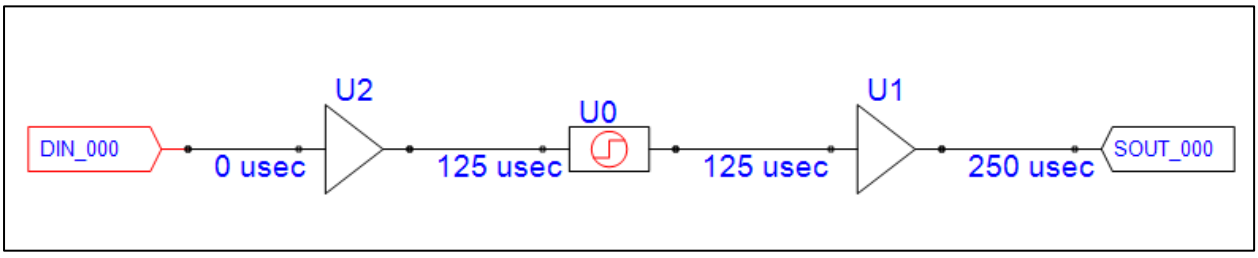


Figure 51 – Timed Interlock Example

A Timer can be embedded into a logic gate through the Properties View. First, select the Timer block in your schematic, then set the Timer Function to a value other than None in the Properties View.

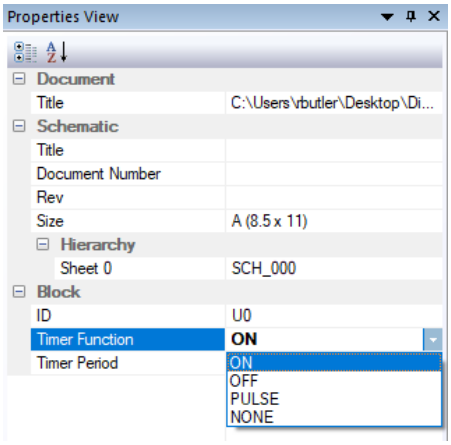


Figure 52 - Setting Timer Function

The DRC checks for some sort of logic before and after timers. Logic gates are not needed before embedded timers but are still required after them.

4.5.2 Timer Period Properties

The Timer Period for a Timer block is also set through the Properties View. The following units can be used to specify the Timer Period and multiple units can be combined.

- Hours
- Minutes
- Seconds
- Milliseconds (msec)
- Microseconds (usec)

Values for the Timer Period setting can include integer or floating-point values and has a resolution of 125 microseconds. The maximum Timer Period is: 9 hours, 19 minutes, 14 seconds, 431 msec, 875 usec.

Examples:

- 10 sec
- 5 hrs 20 sec 125 usec
- 1.2 min 0.2 msec

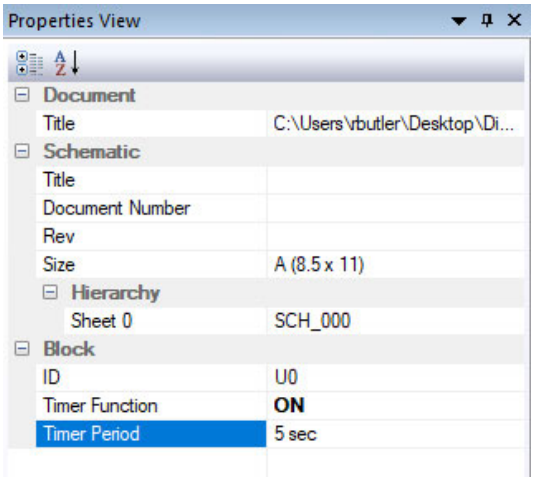
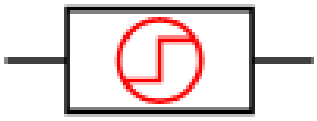


Figure 53 - Setting Timer Period

4.5.3 Timer ON Details



The Timer ON function sets its output to TRUE a specified time after a rising edge on its input. If a falling edge occurs on the timer's input before the timer period elapses, then the timer's output remains FALSE, and the timer's elapsed time is reset to 0.

Figure 54 - Timer ON Function shows the timer's output (Q) as a function of the input (IN) state, elapsed time (Tcnt), and the user-defined timer period (Tp).

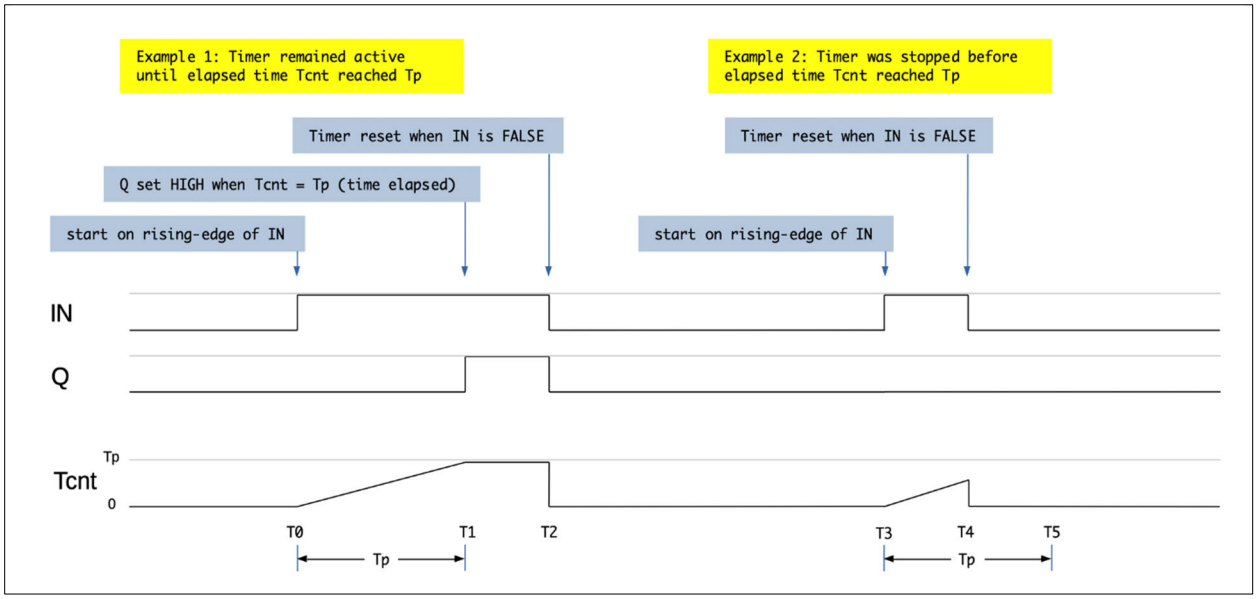
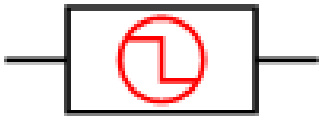


Figure 54 - Timer ON Function

4.5.4 Timer OFF Details



The Timer OFF function sets its output to FALSE a specified time after a falling edge on its input. If a rising edge occurs on the timer's input before the timer period elapses, then the timer's output remains TRUE, and the timer's elapsed time is reset to 0.

Figure 55 - Timer OFF Function shows the timer's output (Q) as a function of the input (IN) state, elapsed time (Tcnt), and the user defined timer period (Tp).

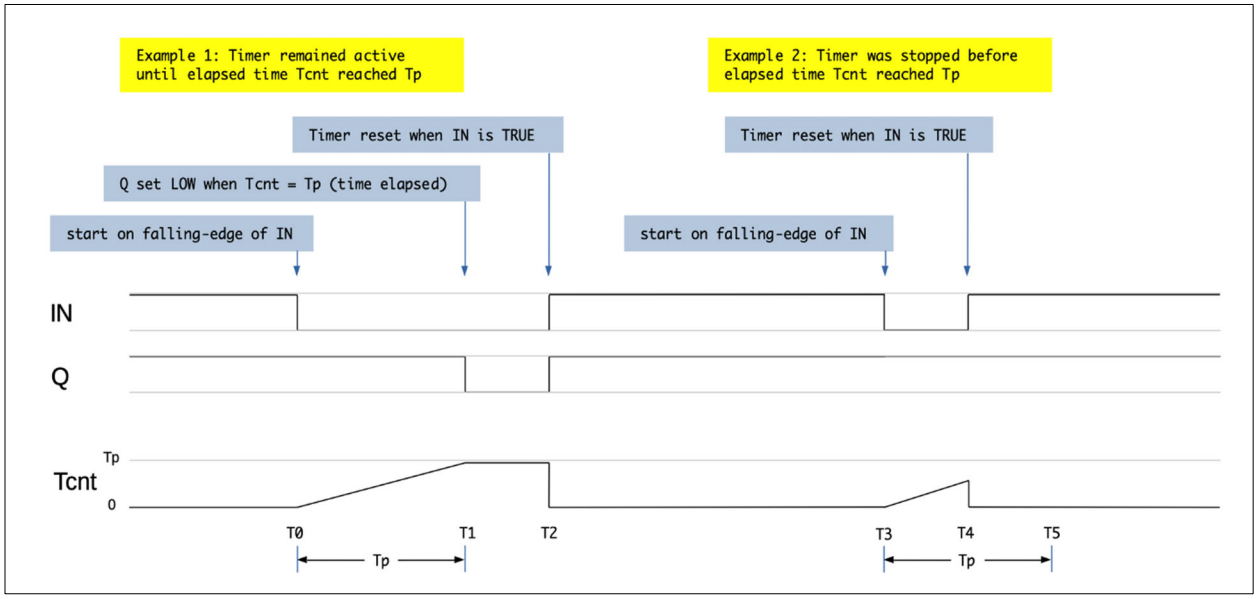
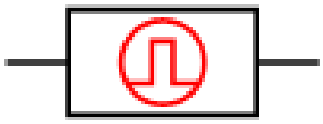


Figure 55 - Timer OFF Function

4.5.5 Timer PULSE Details



The Timer PULSE function sets its output to TRUE for a specified time period after a rising edge on its input. Even if a falling edge occurs mid-way into the pulse period, the timer's output remains TRUE until the pulse period elapses.

Figure 56 - Timer PULSE Function shows the timer's output (Q) as a function of the input (IN) state, elapsed time (Tcnt), and the user defined timer period (Tp).

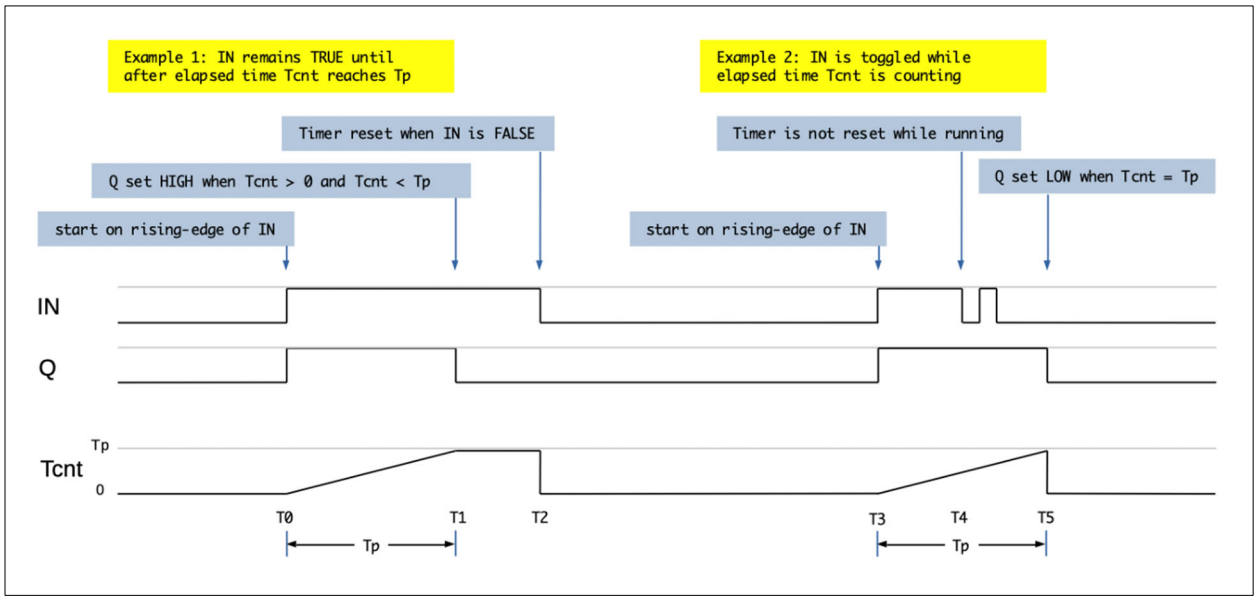


Figure 56 - Timer PULSE Function

4.5.6 Embedded Timers

Select Timer Function other than None in the Properties View Window to turn on the timer in a logic gate. Once a Timer Function is selected, the Timer Period becomes enabled so that you can alter the time to your specifications. Once a Timer Function is switched from None, the timer gets drawn inside the logic gate to represent that it now has an embedded timer associated with it.

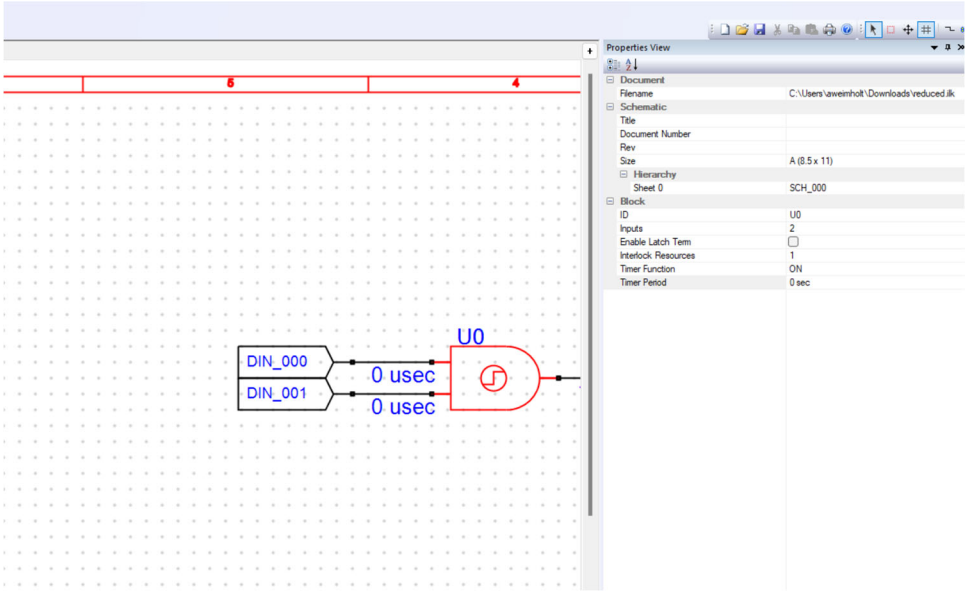


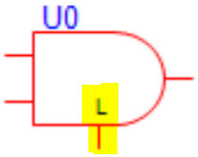
Figure 57 - Embedded Timer

4.6 LATCHES

Interlock Builder provides two types of latching functions which can be used in interlock circuits:

- **Hardware (HW) Latch**
- **Armed Latch**

4.6.1 Hardware Latch



Hardware latches are part of the standard logic gates (Buffer, AND, OR, and XOR) in Interlock Builder.

The hardware latch captures the state of the logic gate's input state on the rising edge of the latch:

- Once the input is latched, the logic gate's output stays TRUE until the falling edge of the input
- When the input goes low, the output stays low until the next rising edge of the latch

Figure 58 - Hardware Latch Behavior shows the behavior of a logic gate's output based on the state of the hardware latch and its input(s).

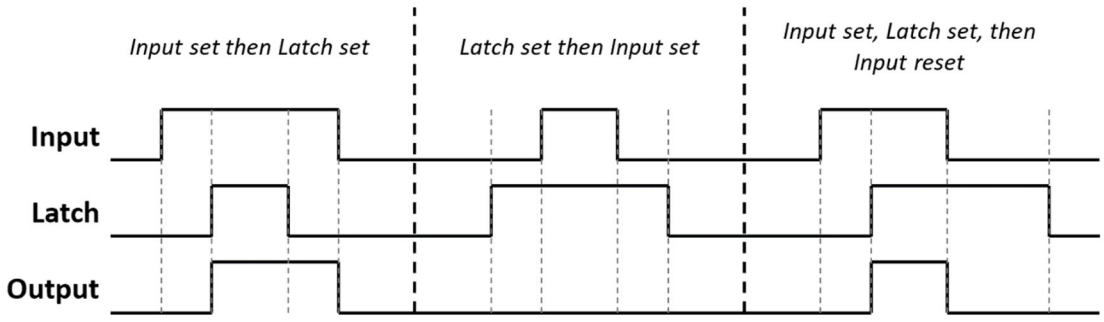


Figure 58 - Hardware Latch Behavior

Enable a logic gate's hardware latch from the Properties View by setting the "Enable Latch Term" property. By default, the latch term is disabled.

Figure 59 - Enable Latch Term Property shows an example of enabling the latch (highlighted) on a logic gate.

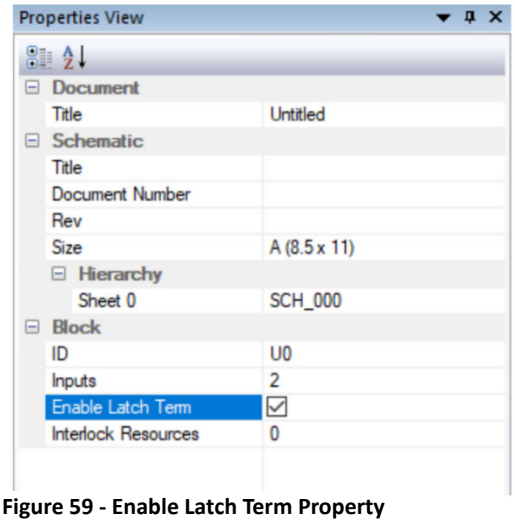
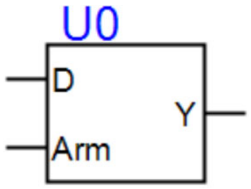


Figure 59 - Enable Latch Term Property

4.6.2 Armed Latch

Armed Latches are schematic blocks with an input (D), output (Y), and latch (Arm) and behaves as follows:



- The output of the Armed Latch is equal to the input (i.e. it is a passthrough) when the latch is FALSE.
- When the latch is TRUE, the output will not change state

This behavior is shown in Figure 60 - Armed Latch Behavior.

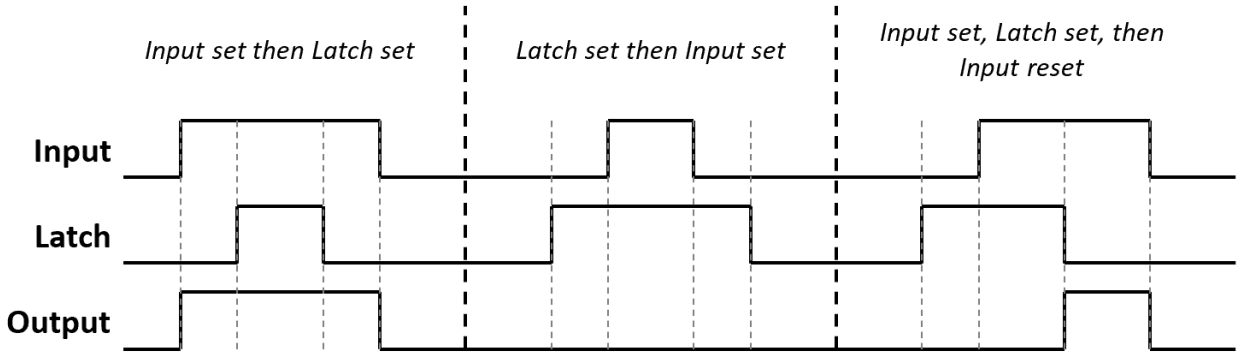


Figure 60 - Armed Latch Behavior

4.7 INTERLOCK PROPAGATION DELAY

Each component in an interlock schematic has a propagation delay associated with it. The cumulative propagation delay at each node in the schematic is calculated and displayed by Interlock Builder. These delays may or may not be negligible, depending on your application.

If it is important that a particular set of input signals be evaluated by an interlock at the same time, then you may insert buffers to equalize the propagation delay of each input's signal path. For example, Figure 62 - Balancing Delays by Adding Buffers shows how buffers would be inserted into Figure 61 - Unbalanced Propagation Delay's schematic to ensure that both inputs to U2 are evaluated simultaneously.

Propagation delays are shown at the output of each logic block. You must account for these delays when designing interlock circuits to avoid unwanted race conditions. This section describes some methods to ensure that signals arrive at critical logic block inputs at the same time, including:

- Adding delays with buffers
- Inverting signals
- Logic design planning

Figure 61 - Unbalanced Propagation Delay shows an example of unbalanced signal propagation delays at the inputs of U2. One input has a 250-microsecond delay from DIN_031 and DIN_032 and the other input has no delay from DIN_033.

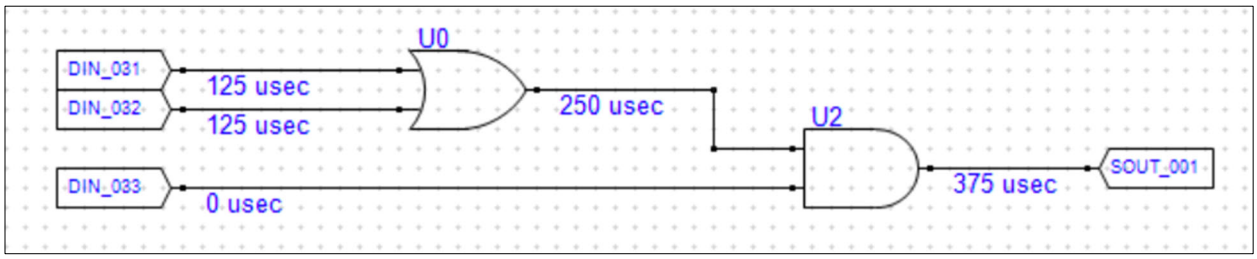


Figure 61 - Unbalanced Propagation Delay

In the above example, an additional 250 microseconds is needed between DIN_033 and U2 to match the propagation delay through OR gate U0.

4.7.1 Adding Delays with Buffers

One method of matching propagation delays is to insert buffers between blocks. Each buffer adds 125 microseconds, so adding (2) buffers between DIN_033 and U2 adds 250 microseconds in this signal path. Figure 62 - Balancing Delays by Adding Buffers shows the same circuit with buffers inserted to the delay needed. Note that each buffer uses an interlock resource.

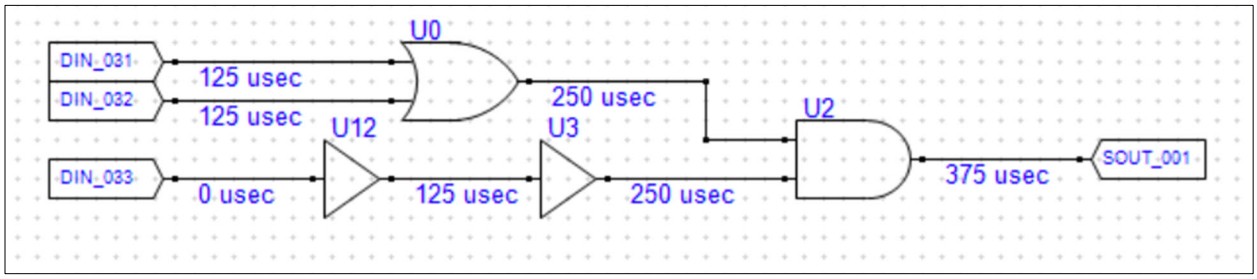


Figure 62 - Balancing Delays by Adding Buffers

4.7.2 Matching Delays by Inverting Signals

Inverting input and output signals at logic gates can add or remove interlock resources needed to implement the Boolean logic and add or remove delays as a result. An interlock design which requires inverted logic, such as Figure 63 - Balancing Delays by Inverting Signals, may utilize this characteristic to help balance out the propagation delays of the interlock circuit.

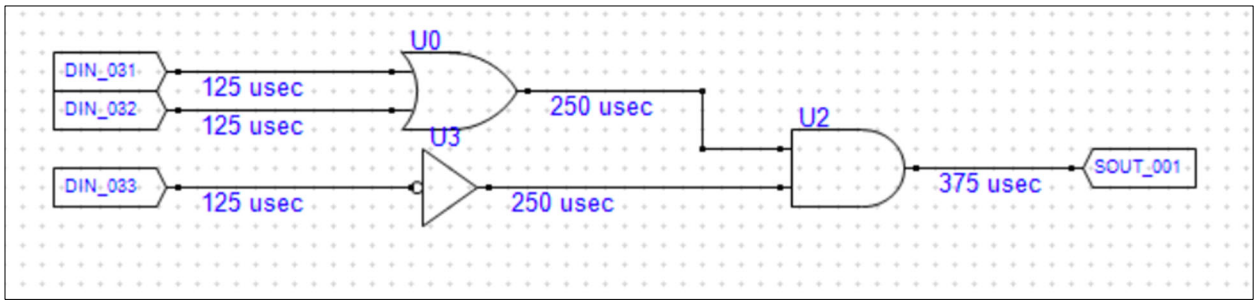


Figure 63 - Balancing Delays by Inverting Signals

4.7.3 Matching with Logic Design

Another method to balance delays is to design circuits with the same number of interlock resources from each DIN to the input pins of timing-critical logic gates. For example, Figure 64 - Balanced Delays by Logic Design has multiple signal paths with different Boolean functions, but all gates have balanced input delays. The SOUTs in this example also have balanced delays.

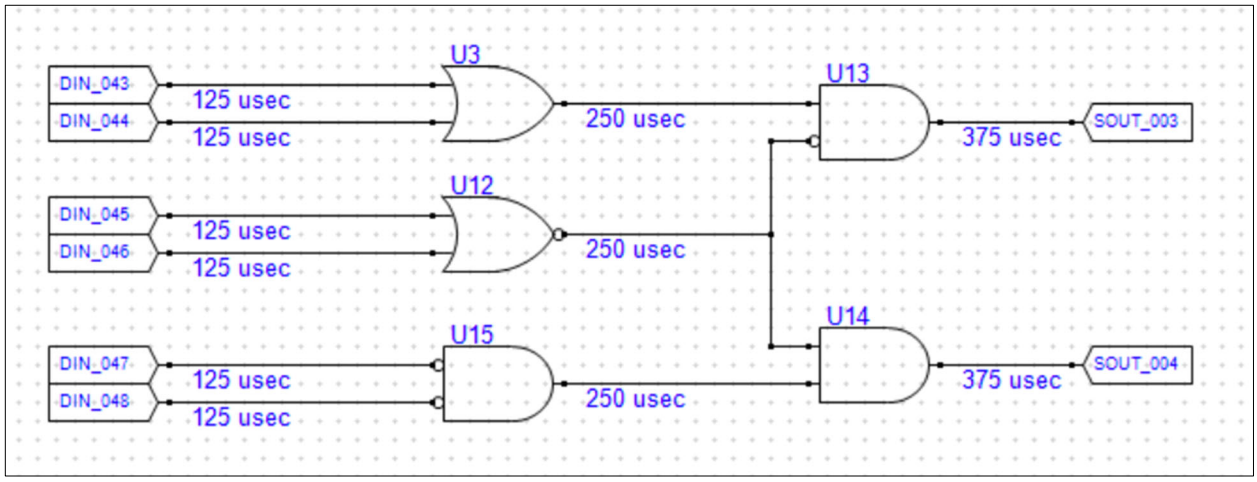


Figure 64 - Balanced Delays by Logic Design

5 INTERLOCK DESIGN TOOLS

Now let's look at how to use the design tools. You can do the following:

- Placing, selecting, and moving schematic blocks
- Inverting pin logic
- Wiring schematic blocks together

5.1 PLACING SCHEMATIC BLOCKS

Schematic blocks (e.g. Logic Gates, IO Ports, and Latches) can be selecting from multiple places in Interlock Builder:

- Schematics Toolbar (Figure 65 - Schematics Toolbar)
- Schematic Menu (Figure 66 - Schematic Menu)
- Keyboard Shortcuts (Table 3 – Keyboard Shortcuts for Schematic Blocks)

Figure 65 - Schematics Toolbar

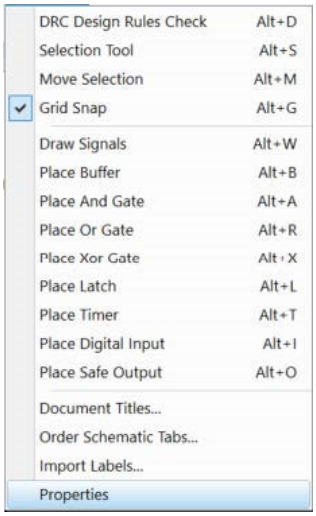


Figure 66 - Schematic Menu

Shortcut	Description
Alt+B	Place a Buffer
Alt+A	Place and AND Gate
Alt+R	Place an OR Gate
Alt+X	Place an XOR Gate
Alt+L	Place a Latch
Alt+I	Place a DIN Port
Alt+U	Place a DOUT Port
Alt+O	Place an SOUT Port

Table 3 – Keyboard Shortcuts for Schematic Blocks

To place blocks:

- By default, multiple blocks can be placed one after another each time the mouse is clicked on the schematic.
- Press the ESC key to exit repeated place block mode.
- To place only a single block on the schematic, double-click the block's toolbar button.

When you place blocks, they snap to the schematics grid. The grid snap toolbar button  enables or disables snap-to-grid mode. When the grid-snap toolbar button is disabled, drawing signals and moving objects may be moved freely.

5.2 SELECTING OBJECTS

Select one or more objects before moving or deleting schematic objects (e.g. blocks & wires) or editing a block's properties. Tools available in Interlock Builder allow you to select both single or groups of objects. When selected, objects are highlighted in RED.

5.2.1 Selecting Single Objects

- Select a single object by clicking it once.
- Deselect the object by clicking outside of it.

5.2.2 Selecting Multiple Objects

Use the Select Objects  mode to draw a window around the objects you want to select. By default, only the objects entirely within the window are selected. Note in Figure 67 - Default Window Selection Mode that the AND gate which is not entirely within the selection window is not selected; all selected objects are highlighted in RED.

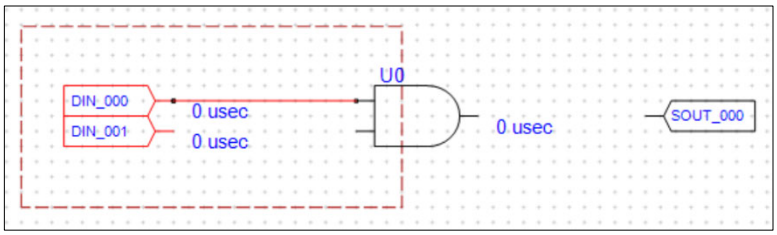


Figure 67 - Default Window Selection Mode

Press the SHIFT key while drawing the selection window to allow any objects which the window crosses to be selected.

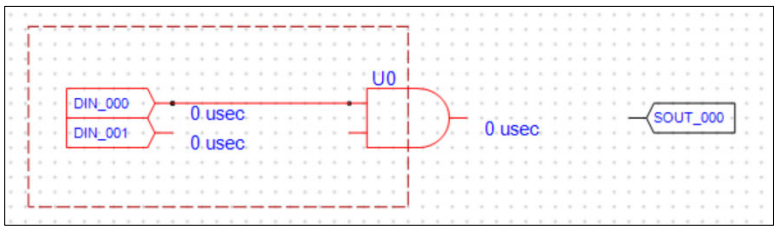


Figure 68 - Window Selection Crossing Mode

5.2.3 Adding and Deselecting with CTRL Key

Press and hold the CTRL while clicking to add multiple objects to a group. Individual objects which are already in a selection group can be deselected by clicking them while holding down the CTRL key.

5.3 MOVING OBJECTS

The Edit , Move , and Selection buttons can be used to make changes to schematic objects (blocks and wires), such as:

- Moving objects
- Deleting objects
- Setting properties of blocks
- Selecting multiple objects

5.3.1 Moving Single Objects

Single objects can be moved in both Edit and Move modes. Any wires connected to the object remain connected.

1) Select the object to be moved, as shown in Figure 69 - DIN_000 Selected.

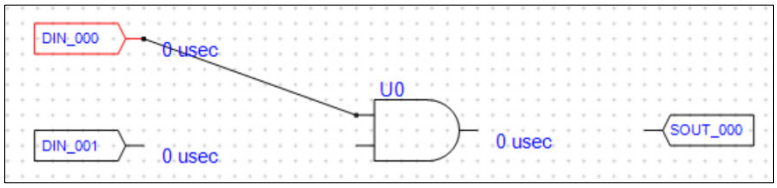


Figure 69 - DIN_000 Selected

2) Click and hold the left mouse button on the selected object and drag it to a new location.

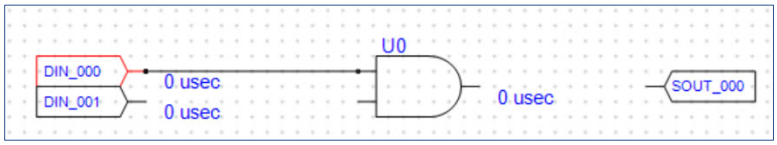


Figure 70 - DIN_000 Moved

5.3.2 Moving Multiple Objects

The Move mode is used to move multiple selected objects by clicking anywhere on the schematic then dragging to the new location. The currently highlighted selection does not change while in the move mode. To change the selected objects, switch back to the edit or selection mode.

5.4 INVERTING PINS

The input and output pins on blocks such as logic gates, timers, and latches can be modified so that their logic is inverted.

To invert a pin on a logic block, double click at the end of the desired pin. On the first click, a large red square will appear at the end of the pin (Figure 71 - Click Location for Inverting a Pin). A second click completes the pin inversion.

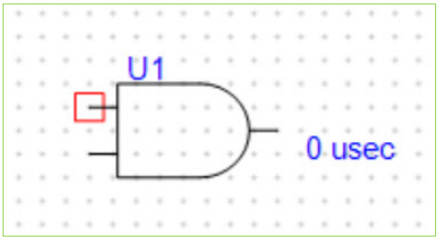


Figure 71 - Click Location for Inverting a Pin

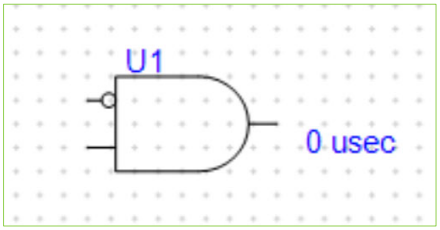


Figure 72 - Pin Inversion Complete

For example, when a digital input (DIN) is connected to a buffer and that buffer's input pin is inverted, the buffer sees a TRUE signal when the DIN is FALSE, and it sees a FALSE signal when the DIN is true.

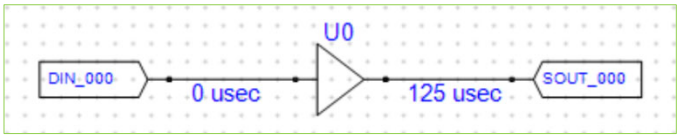


Figure 73 - Buffer with Default Pins

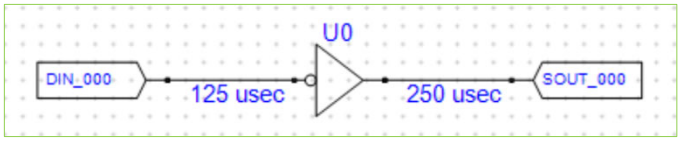


Figure 74 - Buffer with Inverted Input

When the output pin of a logic block is inverted, the results of the logic function are inverted. Figure 76 - AND Gate with Inverted Output shows an interlock with an AND gate which has an inverted output.

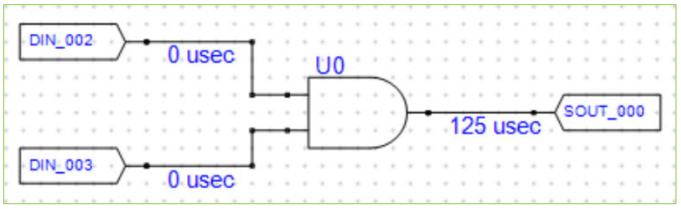


Figure 75 - Interlock with Default AND Gate

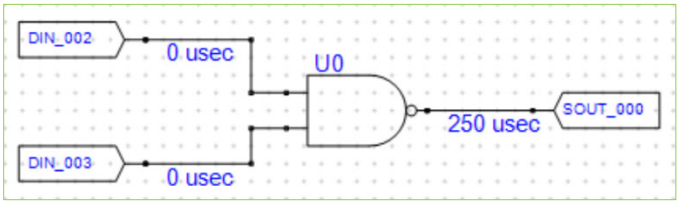


Figure 76 - AND Gate with Inverted Output

The truth table shown in Figure 77 - Truth Table for AND Gate with Inverted Output shows the results of the interlock shown in Figure 76 - AND Gate with Inverted Output, where the AND gate's output is inverted.

Input 1	Input 2	Output
0	0	1
0	1	1
1	0	1
1	1	0

Figure 77 - Truth Table for AND Gate with Inverted Output

5.5 WIRING BLOCKS

Schematic blocks can be connected with wires in both Edit mode and Wire mode. These modes can be selected from the toolbar, the Schematic menu, or with keyboard shortcuts. By default, wire segments snap to the schematics grid. The snap-to-grid mode can be disabled with the grid snap toolbar button  .

Toolbar Buttons

- Wire mode: 
- Edit mode: 

The following examples show how to make simple connections between blocks as well as how to draw wires which have multiple segments.

5.5.1 Example #1: Simple Connection Between Blocks

This example shows how to make a simple connection between two blocks:

1) Left-click the first block's pin. A large red rectangle is shown if the cursor is on a valid connection point (Figure 78 - Starting a New Connection).

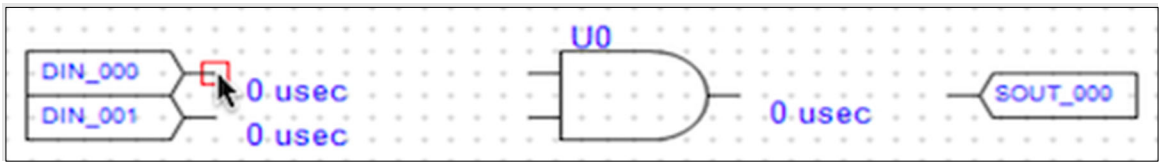


Figure 78 - Starting a New Connection

2) While holding the left mouse button, move the cursor to the next pin to connect. A large red rectangle is shown if the cursor is on a valid connection point (Figure 79 - Locating Next Connection Point).

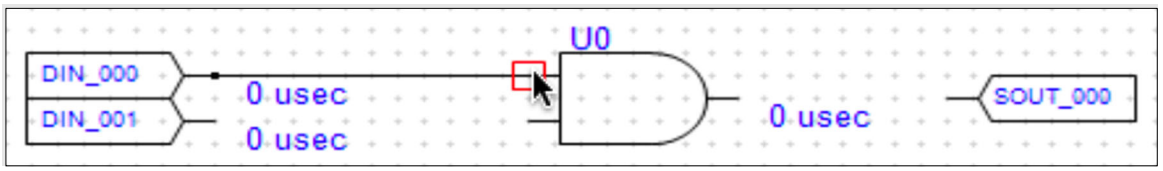


Figure 79 - Locating Next Connection Point

3) Release the mouse button to finish the connection. The new connections at each pin are shown as black vertex points (Figure 80 - Finishing the Connection).

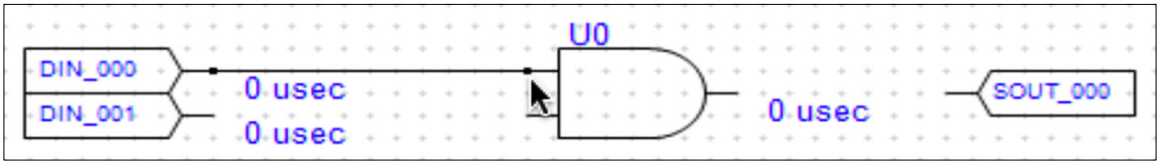


Figure 80 - Finishing the Connection

5.5.2 Example #2: Drawing Multiple Wire Segments

Multiple wire segments can be drawn one after another by holding the Shift key while drawing wires. This can be helpful when making horizontal and vertical segments to connect blocks together.

1) Start a new wire by left clicking on the IO Port pin (Figure 81 - Start of 1st Segment).

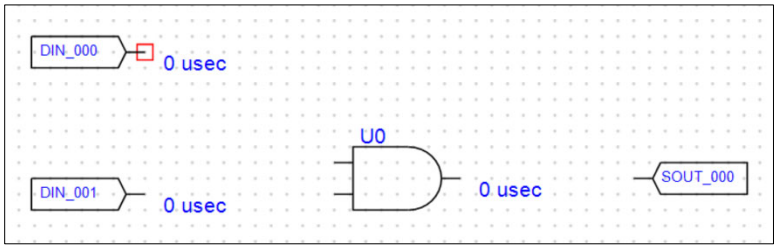


Figure 81 - Start of 1st Segment

2) Move the cursor to the end of the current segment and release the mouse button (Figure 82 - Finish 1st Segment).

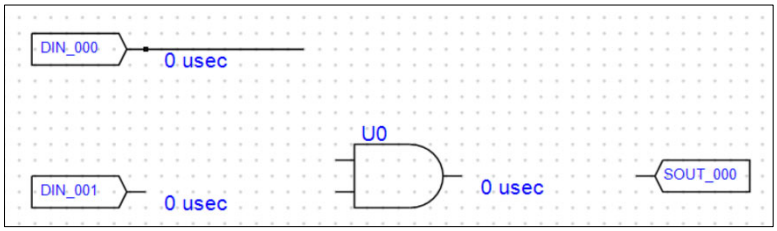


Figure 82 - Finish 1st Segment

3) Start the next segment by holding down the Shift key then clicking on the end of the previous segment (Figure 83 - Start of 2nd Segment).

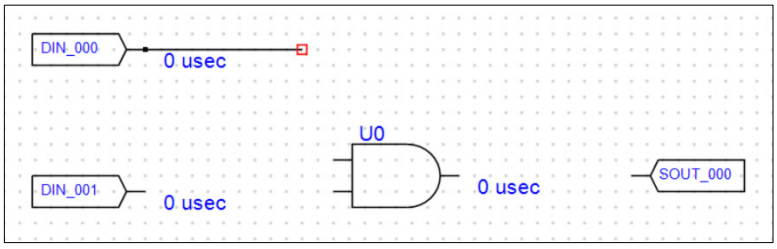


Figure 83 - Start of 2nd Segment

4) Finish this segment by releasing the mouse button (Figure 84 - Finish 2nd Segment).

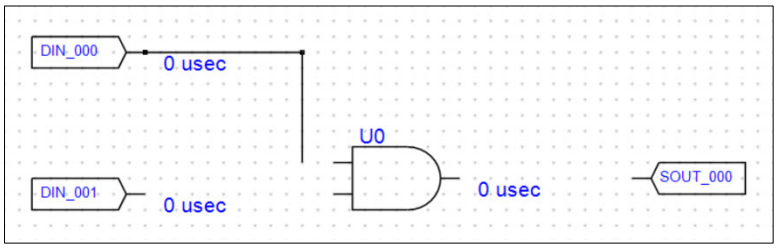


Figure 84 - Finish 2nd Segment

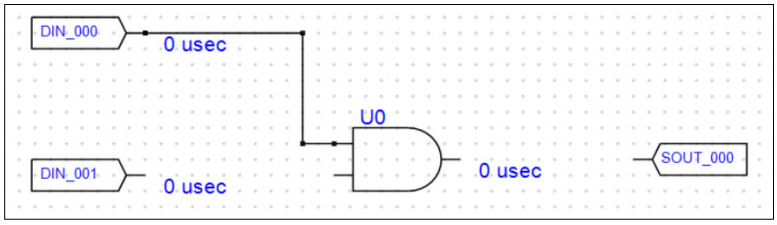


Figure 85 - All Segments Completed

5) Repeat steps 2 & 3 for new segments until a connection to the next pin is made (Figure 85 - All Segments Completed).

5.5.3 Deleting Wire Segments

Wire segments can be deleted while in Edit mode 

1) Select the wire segment to be deleted. The segment is highlighted once it is selected.

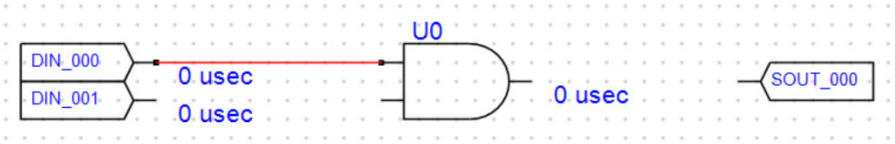


Figure 86 - Wire Segment Selected & Highlighed

2) Press Alt+D or the Delete key to delete the wire.

6 PROGRAMMING INTERLOCKS

Program interlocks into Fusion.IO system by pressing the Program button.

1) Ensure that the PC is connected to the Fusion device's LAN port via Ethernet and that the PC has an appropriate static IP address.

   Note: *Fusion devices have a default IP address of 192.168.9.50. So, a typical static IP address for the PC would be 192.168.9.X ('X' is any number between 0-255 except for 50).*

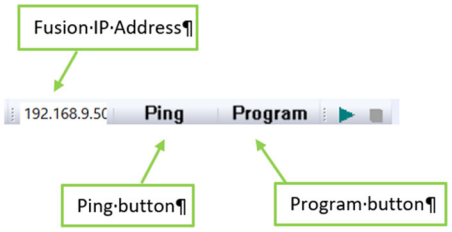


Figure 87 - Programming Toolbar

2) Test communication with the Fusion device by clicking the Ping button. The Log View shows "Ping Success" if communication is successful.

3) Once communication has been verified, click "Program" to download the interlock(s) into the Fusion device.

4) When programming starts:

   - The Fusion device chirps one time.
   - Interlock Builder displays a "Programming in progress" dialog (Figure 88 - Programming in Progress).
   - A progress meter is available in the lower-right corner of Interlock Builder (Figure 89 – Programming Progress Bar).

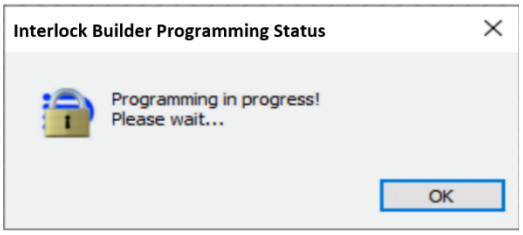


Figure 88 - Programming in Progress

Figure 89 – Programming Progress Bar

5) When programming is complete:
   - The Fusion device chirps three times
   - Interlock Builder displays a "Programming Successful!" dialog (Figure 90 - Programming Successful)
   - The progress meter (lower-right corner of Interlock Builder) is at 100%

6) Cycle power on the Fusion device after programming has been successfully completed.

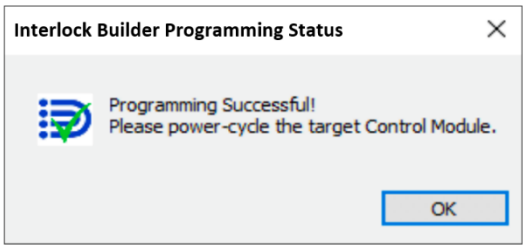


Figure 90 - Programming Successful

6.1 CONFIGURING A SAFE ANALOG CARD

Large signal safe analog cards are analog input cards that allow you to set digital filters, high and low temperature thresholds, etc.

The Large Signal Safe AIN slot card works within the Fusion.IO safety system. It provides up to 8 channels of safe (i.e. SIL-3 under IEC61508) voltage or current measurements.

You can specify which type of sensor you are using by specifying if the connected sensor is a thermocouple sensor (TC) or resistance temperature detector sensor (RTD), and which subtype of sensor it is. This changes how the raw data is converted to temperature to be displayed over ECAT (data is shown in units of 1/16 degree C). You can also enable notch and low-pass filters (set via Filter Bandwidth) and set upper and lower temperature thresholds. An error is posted to the ECAT exception tree to notify you if the temperature goes above or below those set points. There are also per-channel errors raised if there are open or short circuits detected on the pin. These bits are mapped to virtual DINs, which can be seen in slot n+24 and are listed in the Properties View of the specific Safe Analog In (SAI) channel.

To use the status DINs in interlocks, navigate to the SAI channel to be monitored, reference the desired mapped status section to get the corresponding channel ID, and place a DIN block with that channel ID. There is also a card-wide ADC Self-Test error raised if the set value and the readback checked value don’t match.

To configure each safe analog input channel individually, open the safe analog input card by navigating to desired channel within the System View tree pane control.

The Properties View is updated with safe configuration information that can be edited for that specific channel.

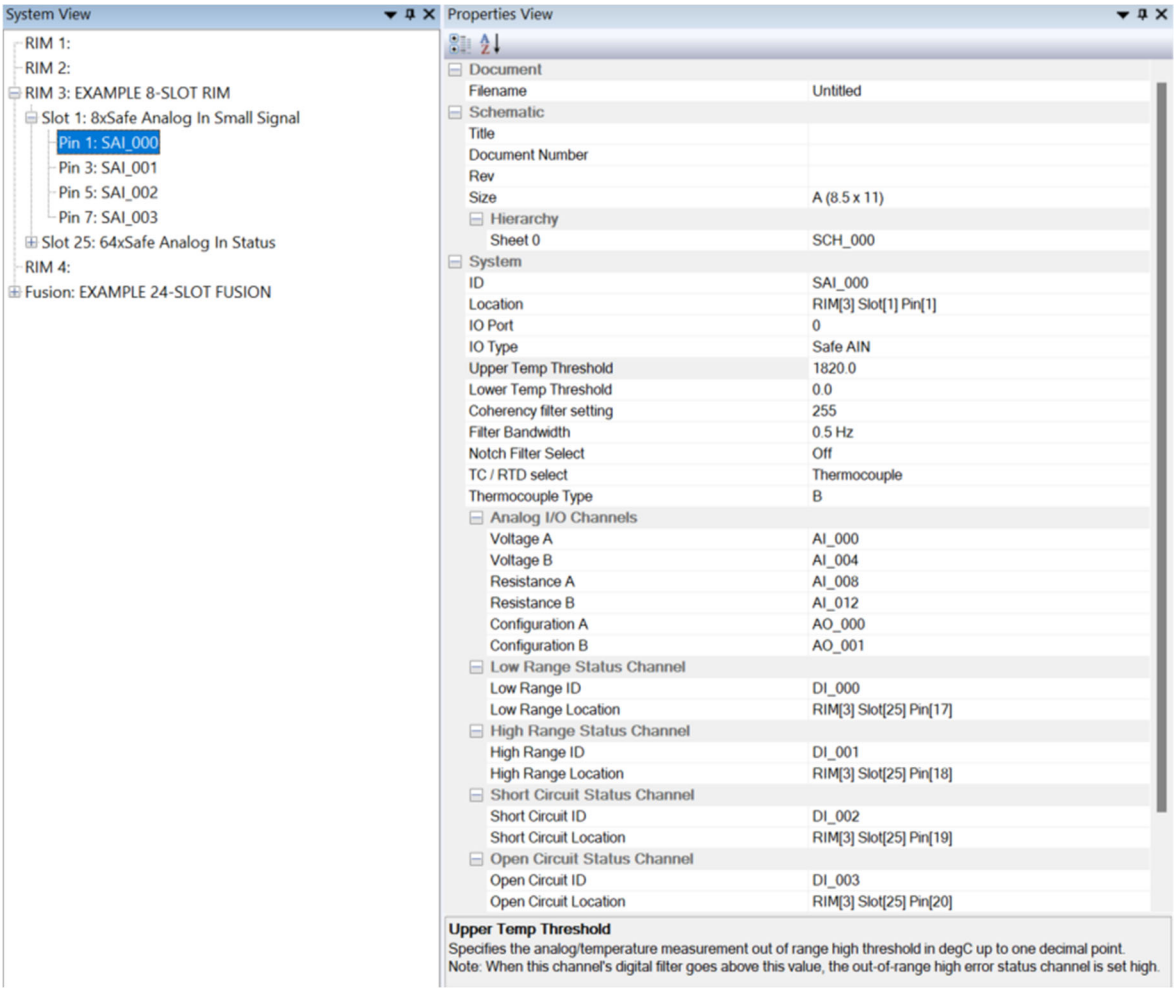


Figure 91 - Configure Safe Analog Card

The listed channels seen in each safe analog channel refer to the locations of the corresponding reading, status, or configuration channel.

6.2 TROUBLESHOOTING PROGRAMMING ERRORS

If programming was not successful, here are examples of error messages that Interlock Builder provides which indicate the issue which prevented programming:

- "Ping failed" message is shown in the Log View. Communication with Fusion.IO system was not possible.

Figure 92 - Ping Failed

Possible Causes & Solutions:

- Ethernet cable is physically disconnected between the computer and the Fusion device
  - Verify that the Ethernet cable is plugged in between the computer and the Fusion device.

- When the cable is properly connected, the green Link LED on the Ethernet ports (Figure 93) of both the computer and the Fusion device is either solid or flashing. Clicking “Ping” in Interlock Builder (Figure 87) causes this LED to flash when there is a good connection.

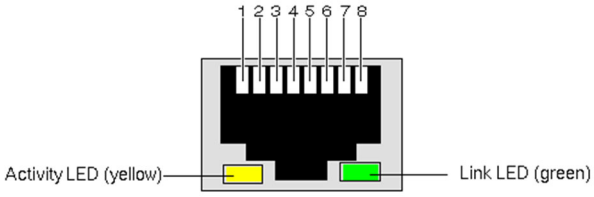


Figure 93 - Ethernet Port LEDs

- IP address on the computer is not set correctly.
  - Verify that the computer has an appropriate static IP address. Fusion devices have a default IP address of 192.168.9.50, so the computer should have an IP address of 192.168.9.xx, where the last digits (octet) can be any number from 1-255 except 50.
  - Verify that the subnet mask on the computer is appropriate. A typical subnet mask is 255.255.255.0, which means that the first 3 sets of digits (octets) of the computer’s IP address must match the Fusion device’s (e.g. 192.168.9 in this example).

- “Target serial number mismatch” message (Figure 94) is shown: Serial number of the Fusion device which is connected to your computer does not match the serial number range in the Interlock Builder system project file.

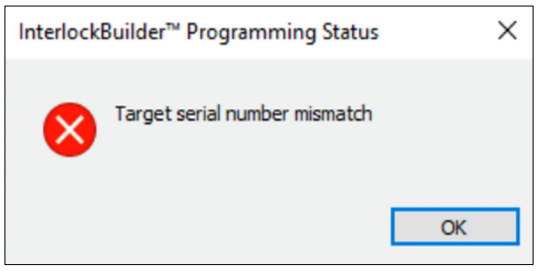


Figure 94 - Serial Number Mismatch

Possible Causes & Solutions:

- The serial number is not listed in the system project file.
- You need to use an updated system project file. Contact the DDI Support / System Engineering team to obtain an updated file. Or if you are using v1.2.3 or later, a single system project file supports any Fusion with the same part number.
- Check the Log Output View pane to see the serial number you tried to program vs the serial number on the actual Fusion unit you are using. Note that the first number is what the Fusion.IO device thinks it is, and the second number is what your system project file is attempting to program.

- Messages about missing buffers or other logical gates before and after timers errors. If an embedded Timer is connected directly to an SOUT, it still needs a buffer in between to initialize it. To ensure that this is clear, the DRC check fails if there exists no interlock term between the embedded Timer and the SOUT.

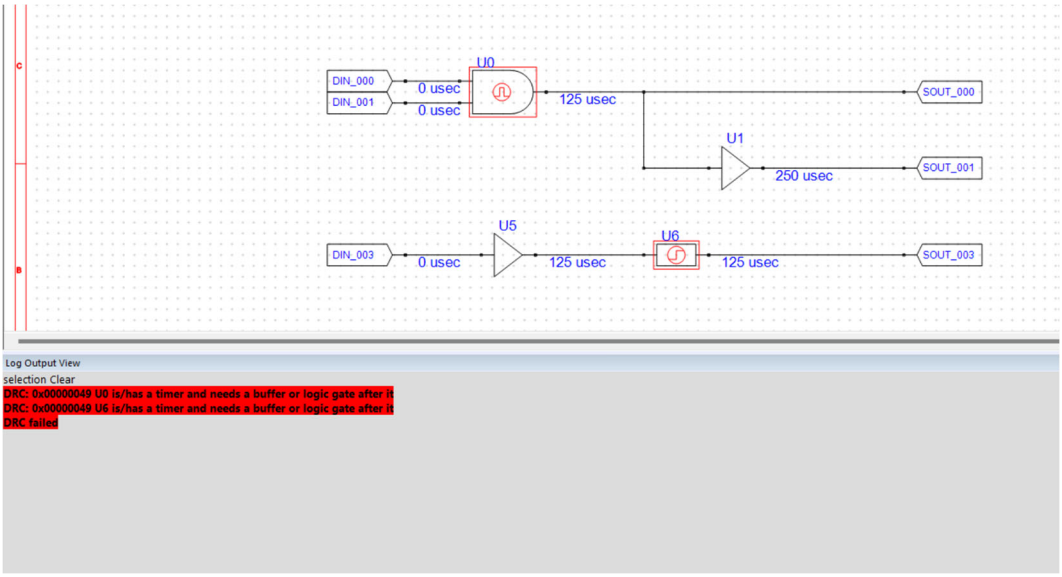


Figure 95 – Log Output showing where buffer or logic gates are needed

Possible Causes & Solutions:

- If you forget to add a logical gate BEFORE the timer, you will see the DIN that is driving the timer affected by the timer functionality. So, for example, if a DIN goes high in the real world, the signal only goes high once the timer period has ended.
- If you forget to put a logical block AFTER the timer, the timer will not be initialized, and the schematic acts as if there is no timer block there. Both behaviors are caused by the need of the logical block's propagation time within the timer.
- If the Interlock logic does not cause the SOUT term to go high, even when the required signals are asserted. Double check that the EtherCAT DOUT-paired control is enabled/disabled within the Properties view of the SOUT block as required.

7 FILE AND PRINT FUNCTIONS

7.1 SAVING AND OPENING PROJECTS

System project files can be opened and saved from the File menu (Figure 96 - File Menu) and with the following toolbar buttons or hot keys:

- Open Project:  Open (CTRL+O)
- Save Project:  Save (CTRL+S)

Use File > Open Recent to select from the four most recently used files.

Note: *When schematics have been changed but not yet saved, the project name shown on the title bar is marked with an asterisk *.*

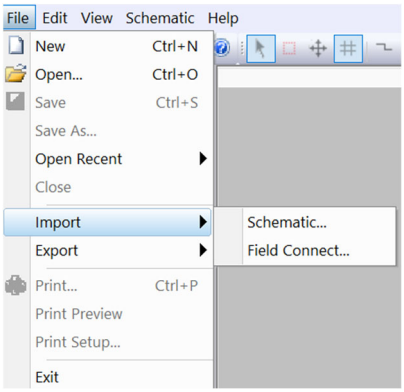


Figure 96 - File Menu

7.2 IMPORTING FILES

Use File > Import > Schematic to import schematic files. Navigate to the file which has a .SCD extension and click Open.

Use File > Import > Field Connect to import field connect files. Navigate to the file which is a .CSV file and click Open. You should see the message that the file imported successfully.

7.3 EXPORTING INTERLOCK FILES

Use File->Export Field Connects to export interlocks from the schematic project as a CSV (comma-delimited) file.

Use File -> Export Schematic As Bitmap to export an image of the schematic project as a BMP (bitmap) file

7.4 PRINTING SCHEMATICS

We recommend that you check the sheet size selected in the schematics' Properties view before printing and set the paper size accordingly. You should also set the orientation to Landscape when printing schematics.

Print schematic sheets using File-> Print or the Print  button.

8 GLOSSARY

These are a combination of Digital Dynamics specific terms and industry standard terms.

Term	Description
Analog Input (AIN)	An analog input style channel which can include -10…+10V, thermocouple, and RTD signals. Analog inputs are not available to be used in Interlocks.
Analog Output (AOUT)	An analog output style channel, for example -10..10V outputs. Analog outputs are not available to be used in interlocks.
Digital Input (DIN)	A digital input channel which can be used as an input term to an interlock
Digital Out (DOUT)	A digital output channel which can be controlled via EtherCAT and can act as an input to an interlock.
EtherCAT	EtherCAT is an industrial ethernet protocol which is suitable for both hard and soft real-time computing requirements in automation technology. EtherCAT is commonly used in machine control, measurement equipment, medical devices, automobiles and mobile machines, as well as in innumerable embedded systems. The EtherCAT Technology Group (ETG) is the standardization organization for EtherCAT and is an official partner of the IEC. Both EtherCAT and Safety over EtherCAT are IEC-Standards (IEC 61158 and IEC 61784).
EtherCAT master	EtherCAT master is the host device in an EtherCAT network which is responsible for managing network activity such as configuration, frame transmission, time synchronization, etc. It is typically a combination of an EtherCAT master stack and computing hardware which includes an Ethernet port.
Functional Safety	The overall safety that depends on a system or equipment operating correctly in response to its inputs. In the case of interlocks designed in Interlock Builder for a Fusion.IO system, functional safety means that the safety interlock operates in accordance with the logic designed via Interlock Builder
Fusion	A Fusion device is the main device used in a Fusion.IO system. It connects to the EtherCAT network and is where Remote Interface Modules (RIMs) are connected. The Fusion device also provides field connections to I/O channels through its onboard slot cards and field connect interface.
PL	Performance Level (PL) is a rating used to define the ability of safety-related parts of control systems to perform a safety function under foreseeable conditions and are correlated with the probability of dangerous failures per hour. The EN/ISO 13849-1 machine safety standard defines Performance Levels a, b, c, d, and e where PL e correlates with the lowest probability of dangerous failures per hour and PL a with the highest.
RIMs	A RIM, or Remote Interface Module, is an I/O expansion module which can be located remotely from the Fusion device and connects to the Fusion device via a redundantly monitored, safety certified serial bus. I/O channels on a RIM are updated in real-time along with a Fusion device's I/O channels and can be combined with

	Fusion I/O channels in safety interlocks.

Safety	Safety is defined as the freedom from unacceptable risk of physical injury or of damage to the health of people, either directly, or indirectly as a result of damage to property or to the environment.
Safety Digital Output (SOUT)	A safety digital output (SOUT) is a digital output channel that can be controlled as the output of a programmed interlock as well as by an EtherCAT master.
SIL	Safety Integrity Level, or SIL, is the likelihood of a system's safety function being performed satisfactorily and is measured in terms of probability of failure. IEC 61508 defines four SIL levels: SIL 1, SIL 2, SIL 3, and SIL 4. A higher number means better safety performance, such as lower probability of failure.
TÜV	TÜV is a testing and certification organization which ensures that a product, service, or process has been tested for safety and that it complies with the requirements of national, regional, and international regulations.